

Platform : Sandy Bridge(PROCESSOR)+Couagr Poinrt(PCH)



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31. DC IN/MDC/BT/D-Resistor
32. HDMI (CH7318B)
33. CPU CORE (ISL62881)
34. +1.5VS(OZ8116)/+0.75VS/+1.8V
35. +1.05VS/+5VA (OZ815)
36. BATT IN/CHARGER(OZ8602)
37. iGPU Core
38. VCC SW/+3.3VA/HIGH-SPEED CAP

M/B Schematic Version Change List

[illegible]

Daughter Board Schematic Version Change List

[illegible]

e/cont= dilma.assiscruz@hotmail.com

Shuttle Inc			
Title A14HV			
Size Custom	Document Number		Rev A
INDEX			
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SYSTEM BLOCK DIAGRAM

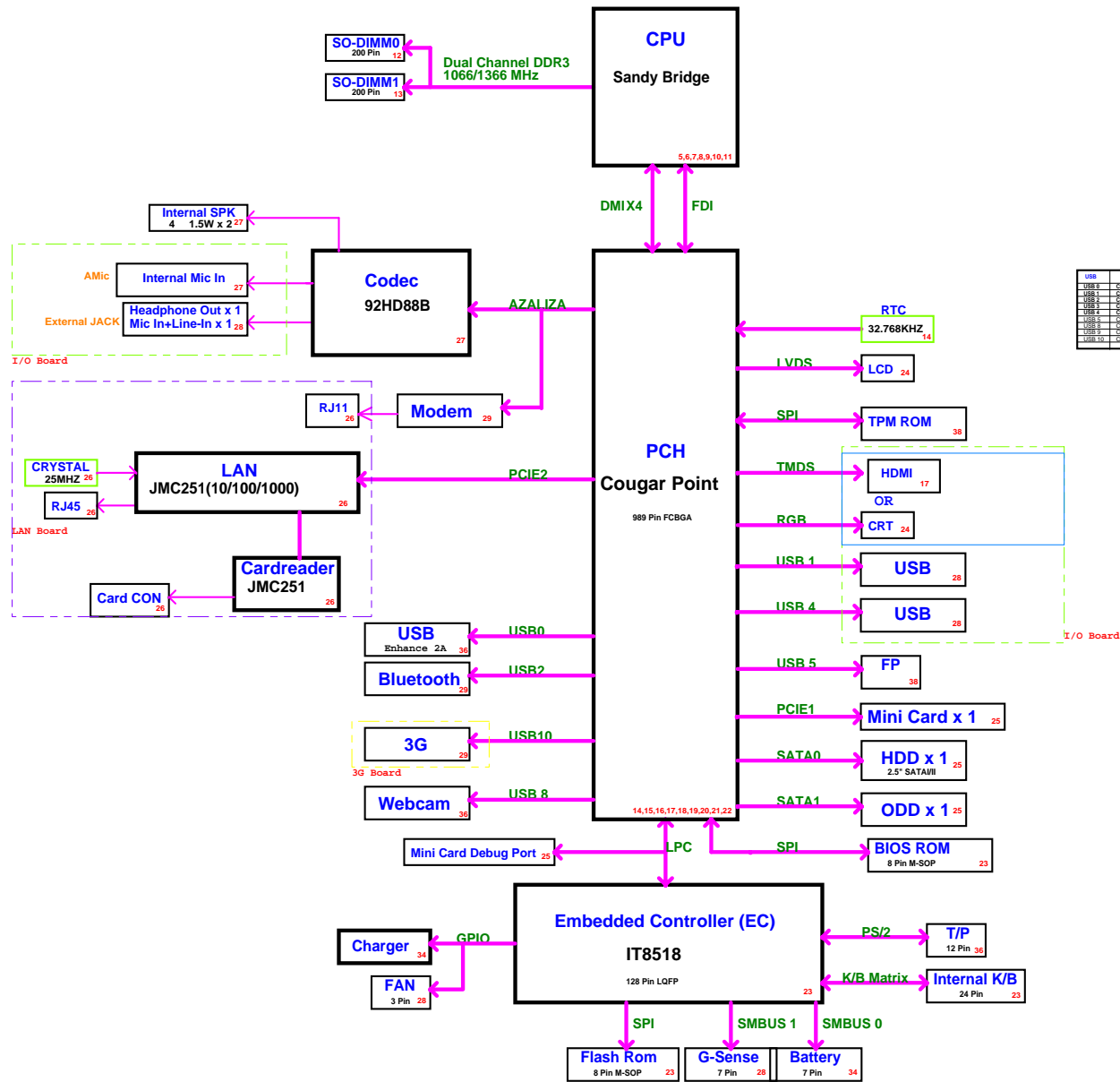


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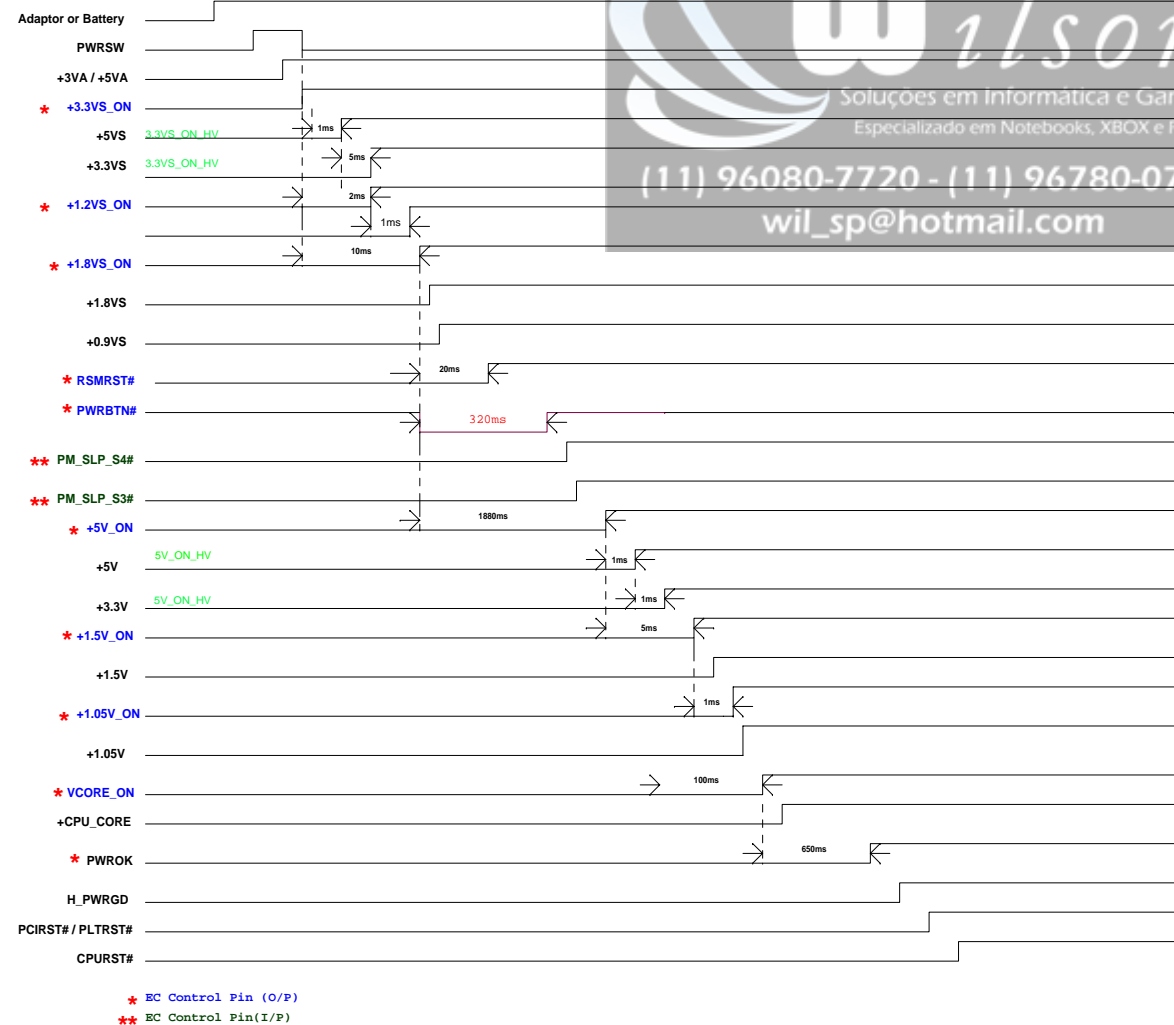
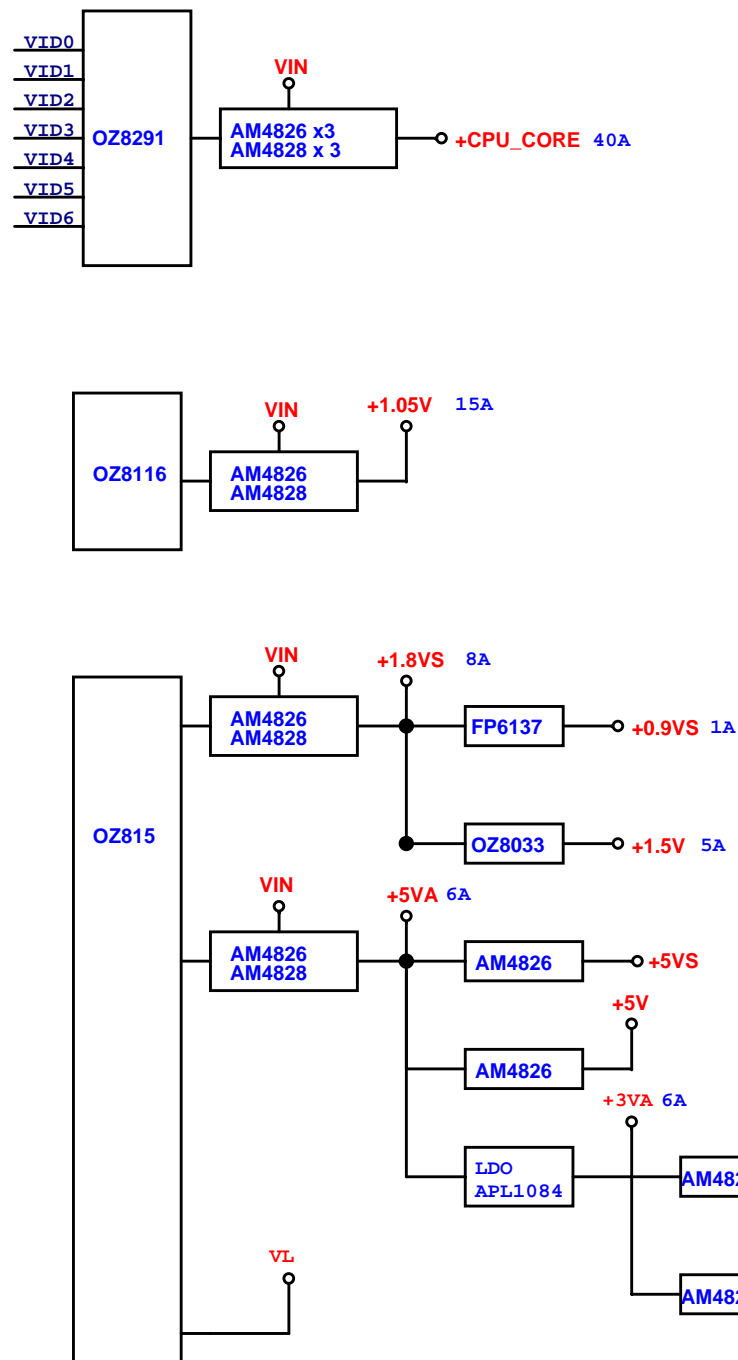
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POWER BLOCK DIAGRAM

System Poewr On Sequence



ICH9M GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQ#
GPIO3	INT_PIRQ#
GPIO4	INT_PIRQ#
GPIO5	INT_PIRQ#
GPIO6	BIOS_REC
GPIO7	N.C (TACH3)
GPIO8	N.C
GPIO9	N.C (WOL_EN)
GPIO10	N.C (ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	N.C (GLAN_DOCK#)
GPIO14	N.C (NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	N.C (TACH0)
GPIO18	N.C
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	N.C (SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	N.C (HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8518 GPIO		Default Pull/Mode
GPA0	PID_3_RF_LED_ON#	UP / GPI
GPA1	BATT_VA_OFF#	UP / GPI
GPA2	BTLL_BEEP	UP / GPI
GPA3	WLAN_PWR#	UP / GPI
GPA4	+1.05V_ON	UP / GPI
GPA5	SENBAT_V	UP / GPI
GPA6	PM_RSMRST#	UP / GPI
GPA7	EC_BL_PWM	UP / GPI
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	3G_PWR#	Dn / GPI
GPB3	SMBCLK	/ GPI
GPB4	SMBDAT	/ GPI
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Funcl
GPB7	SAFTY_PROTECT	Dn / GPI
GPC0	+1.5V_ON	Dn / GPI
GPC1	SMB_CLK_EC	/ GPI
GPC2	SMB_DAT_EC	/ GPI
GPC3	PID_0_CHG_B_LED	Dn / GPI
GPC4	PWRBTN3#	Dn / GPI
GPC5	PANEL_DETECT_2	Dn / GPI
GPC6	VCCSA_ON	Dn / GPI
GPC7	+1.5VS_ON	UP / GPI
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPI
GPD2	PLT_RST#	UP / Funcl
GPD3	PM_SUS_STAT#	UP / GPI
GPD4	EC_EXTSMI#	UP / GPI
GPD5	Fastcharge_EN	UP / GPI
GPD6	+5V_ON	Dn / GPI
GPD7	SET_V	Dn / GPI
GPE0	LID#	Dn / GPI
GPE1	PWR_USB_LED	Dn / GPI
GPE2	ALL_SYS_PGD	Dn / GPI
GPE3	Vcore_ON	Dn / GPI
GPE4	PWRSW	UP / GPI
GPE5	LVDS_VIN	Dn / GPI
GPE6	WLAN_ON	Dn / GPI
GPE7	AMP_MUTE#	UP / GPI
GPF0	PCH_BL_EN	UP / GPI
GPF1	+1.8V_ON	UP / GPI
GPF2	BT_ON	UP / GPI
GPF3	N.C	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	EC PECL	UP / GPI
GPF7	CHG_HI VOLT#	UP / GPI
GPG0	PWRBTN2#	Dn/GPO/TM
GPG1	+3.3VS_ON	Dn/GPO/ID7
GPG2	EC PORST	
GPG6	WEBCAN_ON	Dn / GPI
GPH0	PM_CLKRUN#	Dn/GPI/ID0
GPH1	PID_1_CHG_R_LED	Dn/GPI/ID1
GPH2	PID_2_PWR_LED	Dn/GPI/ID2
GPH3	EC_HSCS0#	Dn/GPI/ID3
GPH4	EC_HSCK	Dn/GPI/ID4
GPH5	EC_HMISO	Dn/GPI/ID5
GPH6	EC_HMOSI	Dn/GPI/ID6

ITE8518 GPIO		Default Pull/Mode
GPI0	CRT_DETECT	/GPI/ADC
GPI1	PANEL_DETECT	/GPI/ADC
GPI2	PLATFORM_ID	/GPI/ADC
GPI3	CPPE#	/GPI/ADC
GPI4	BAT_I	/GPI/ADC
GPI5	BATT_TEMP	/GPI/ADC
GPI6	ADAPTOR_1	/GPI/ADC
GPI7	BAT_V	/GPI/ADC
GPJ0	EC_BL_ON	/GPI/DAC
GPJ1	EC_PROCHOT	/GPI/DAC
GPJ2	FAN_CTRL0	/GPI/DAC
GPJ3	CHG_REF	/GPI/DAC
GPJ4	CHG_I	/GPI/DAC
GPJ5	PWR_USB#	/GPI/DAC

Penryn CPU				
	CPU CORE(V)	ICC(A)	W	TEMP ()
IMVP-6+	1.05	44.0	36	

Cantiga			
VCC	ICC(mA)	W	TEMP ()
+3.3V	262	0.87	105
+1.8VS	3249	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

ICH9M			
VCC	ICC(mA)	mW	TEMP ()
+5V	4	20	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	



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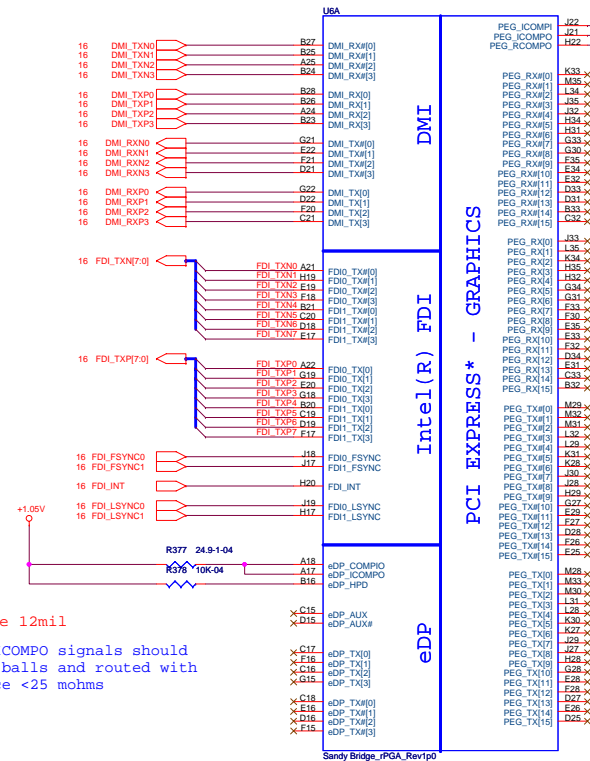
CLOCK GENERATOR			
VCC	ICC(mA)	mW	TEMP ()
+3.3V	1000	3300	70

IDT92HD81			
VCC	ICC(mA)	mW	TEMP ()
+3.3V(DVDD)	200	660	70
+5V(AVDD)	1000	5000	

ADM1032			
VCC	ICC	mW	TEMP ()
+3.3V	170uA	0.56	150

JMC261			
VCC	ICC(mA)	mW	TEMP ()
+3.3VS	300	990	70
+1.2VS	150	180	

SANDYBRIDGE PROCESSOR(DMI,PEG,FDI)



1. PEG_ICOMP1 and RCOMP1 signals should be routed within 500 mils typical impedance = 43 mohms..4mils
2. PEG_ICOMPO signals should be routed within 500 mils..12mils typical impedance = 14.5 mohms
3. spacing to other 15mils

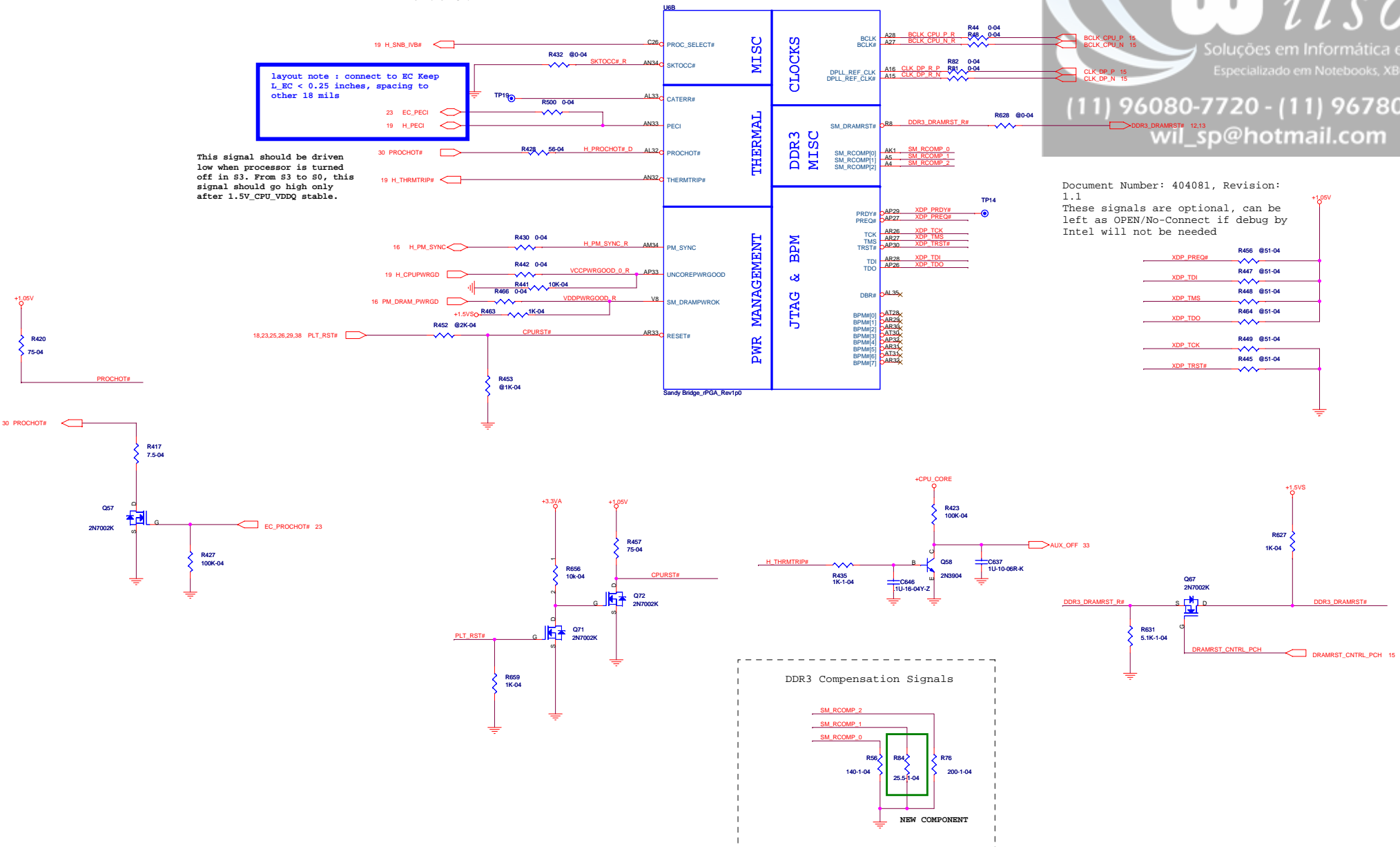


SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)

This pin is for compability with future platforms. A pull up resistor to VCPLL is required if connected to the DF_TVS strap on the PCH.

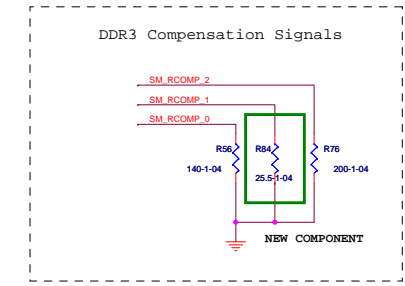
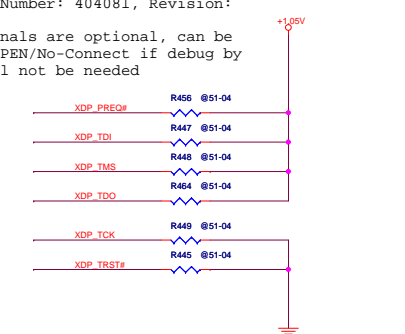
layout note : connect to EC Keep L_EC < 0.25 inches, spacing to other 18 mils

This signal should be driven low when processor is turned off in S3. From S3 to S0, this signal should go high only after 1.5V_CPU_VDDQ stable.

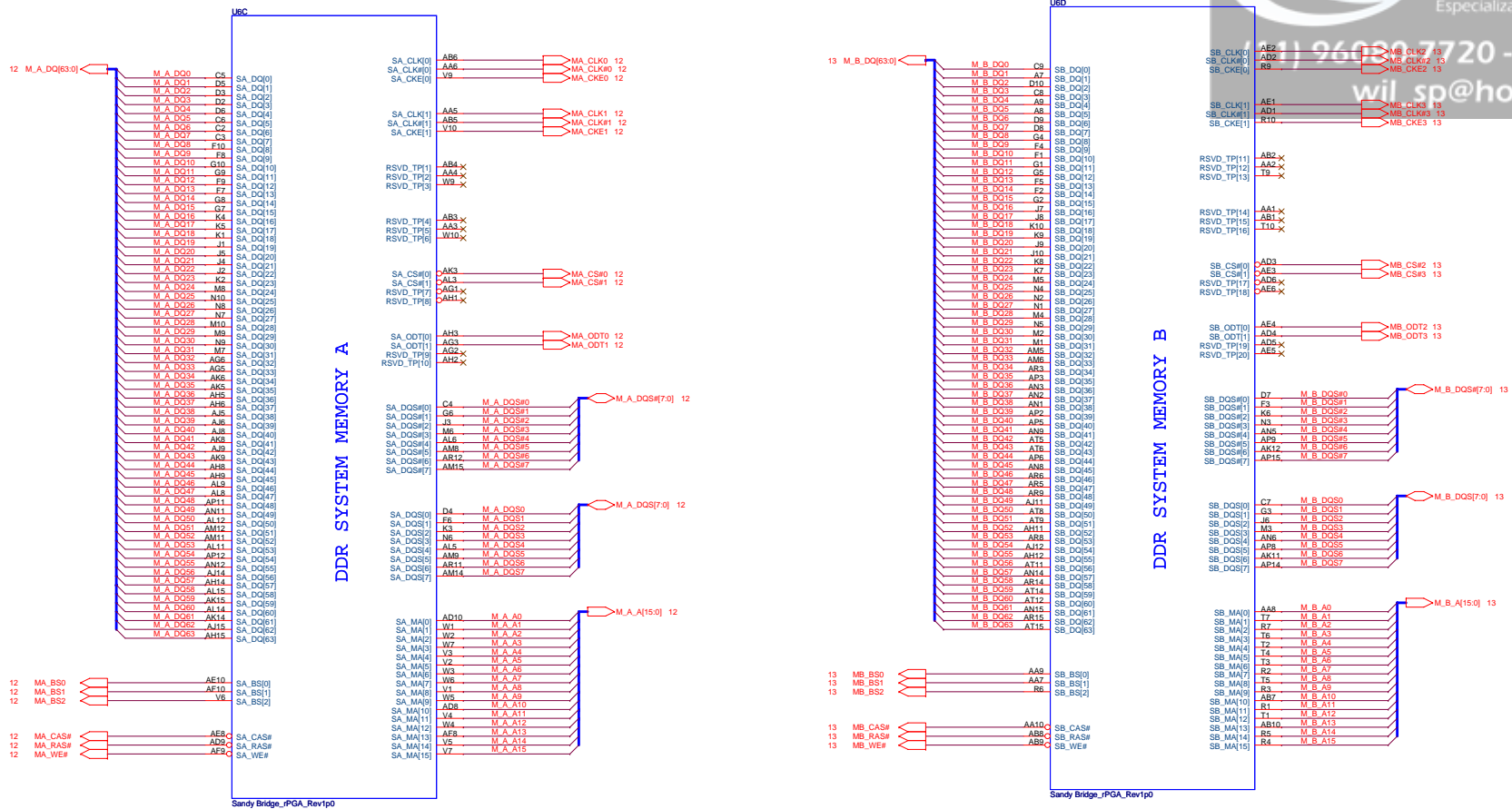


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Document Number: 404081, Revision: 1.1
These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed



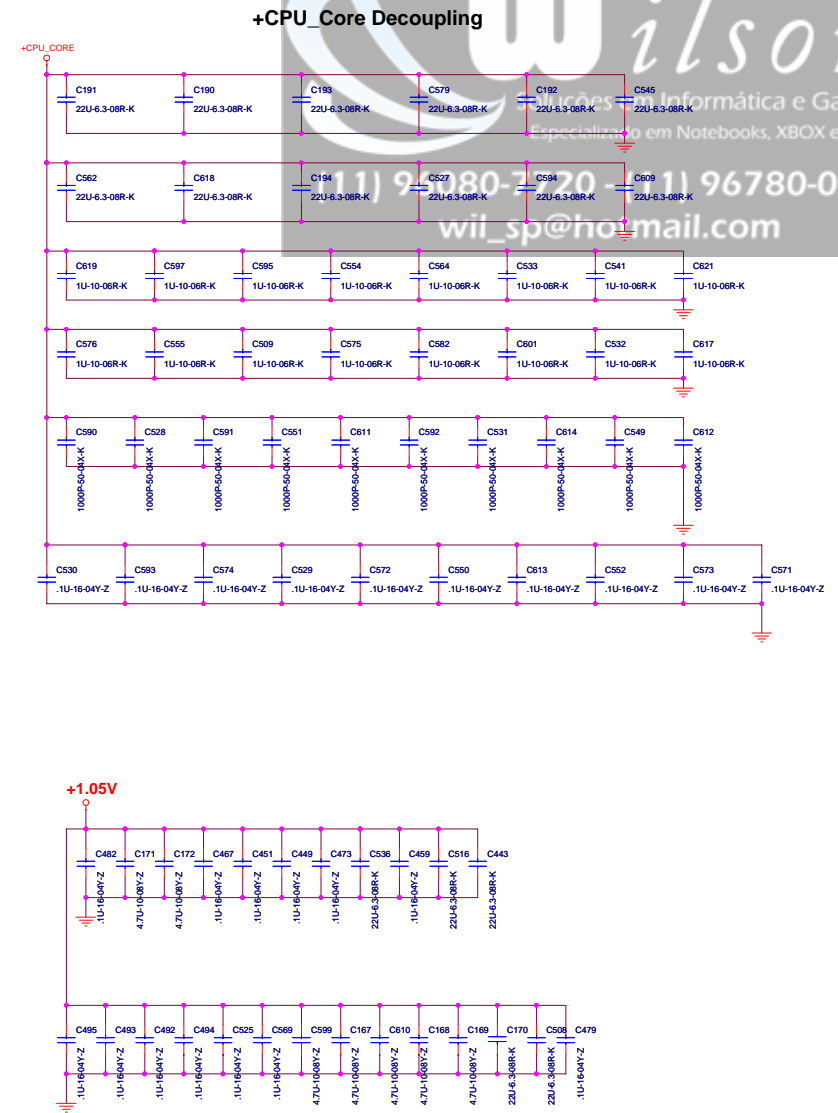
SANDYBRIDGE PROCESSOR (DDR3)



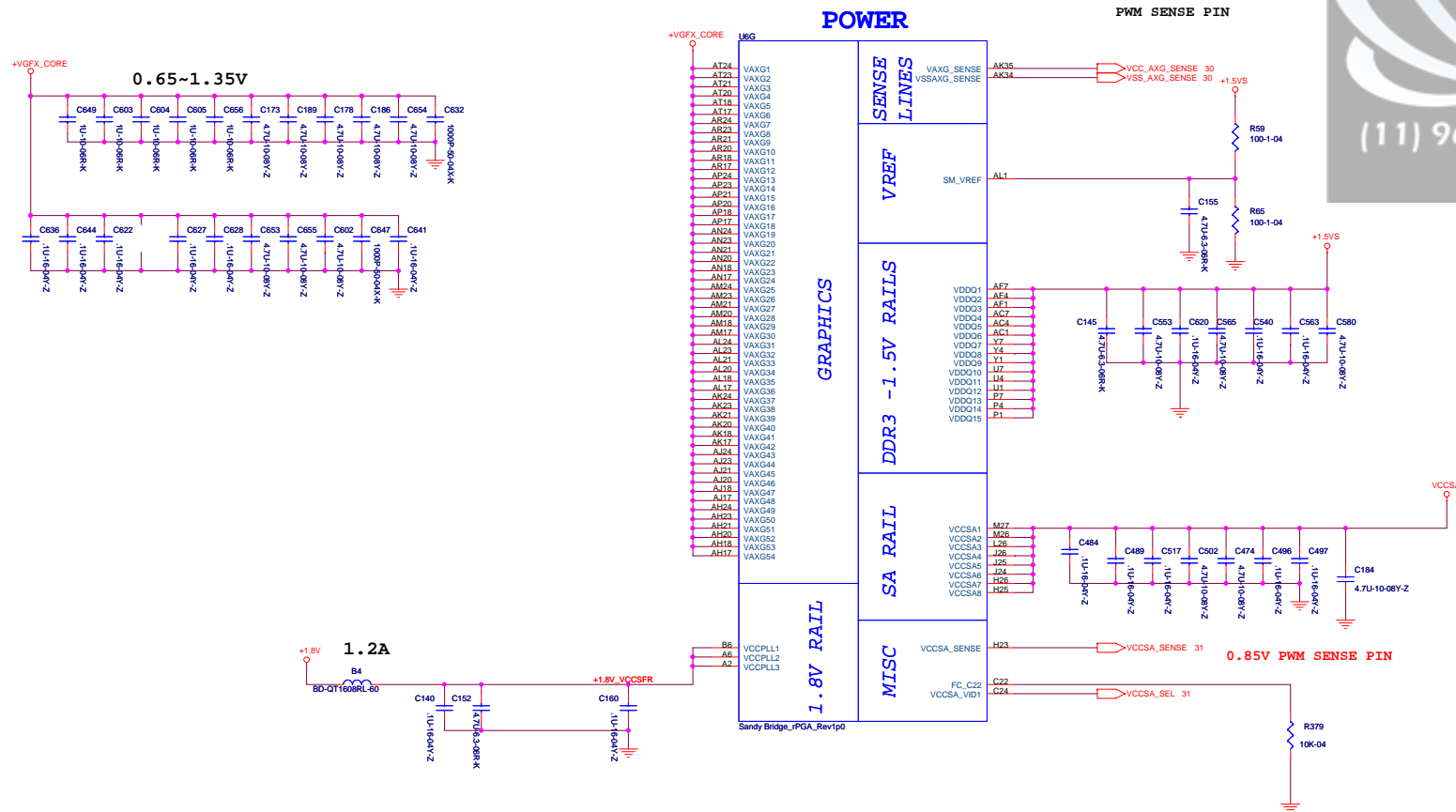
Sandy Bridge_PGA_Rev1p0

Sandy Bridge_PGA_Rev1p0

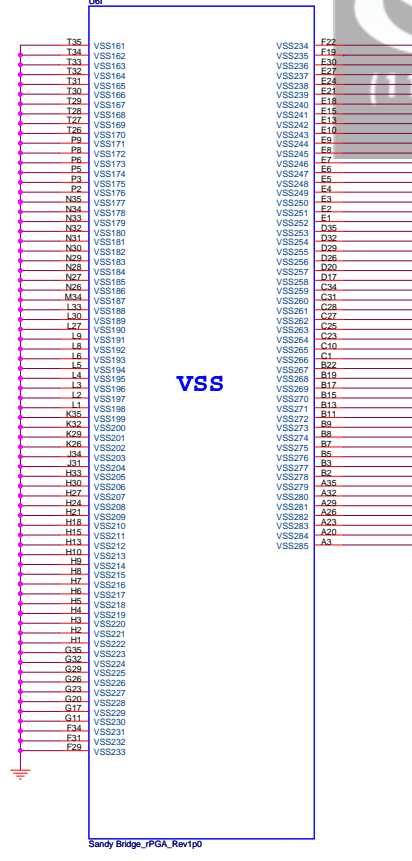
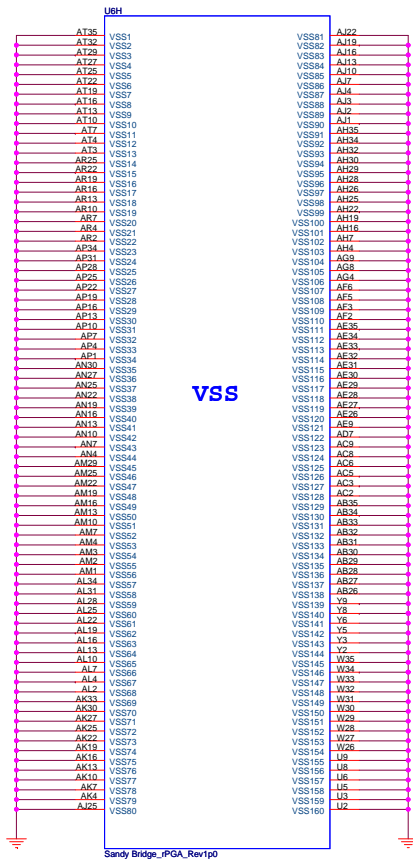
CPU_Core Decoupling



SANDYBRIDGE PROCESSOR (POWER)

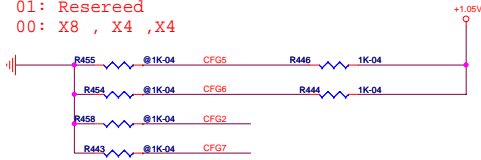


SANDYBRIDGE PROCESSOR (VSS)

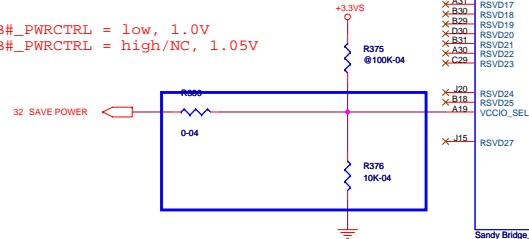


SANDYBRIDGE PROCESSOR (RESERVED)

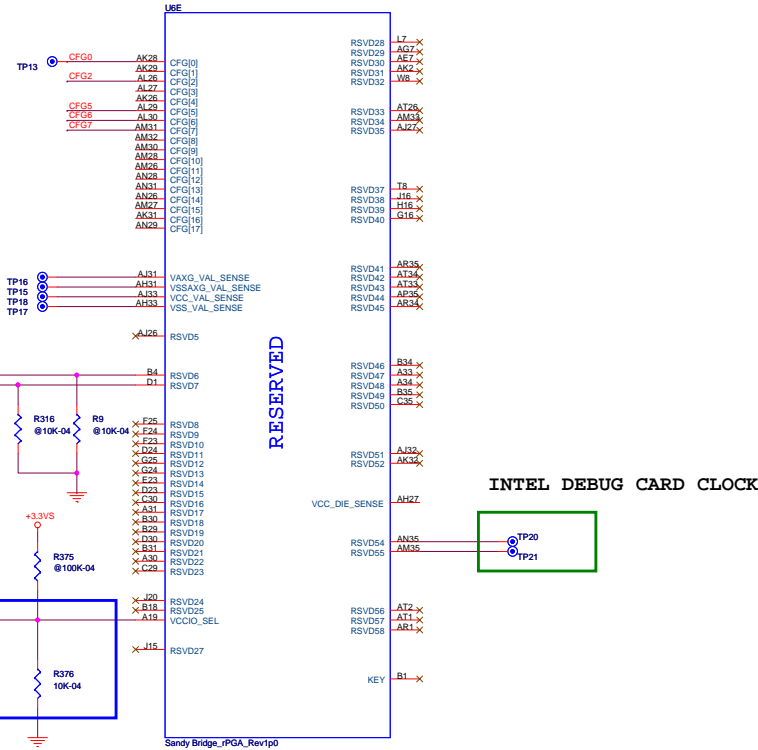
PCIE Port Bifurcation Straps
CFG[6:5]
11: (Default) X16
10: X8 , X8
01: Resereed
00: X8 , X4 ,X4

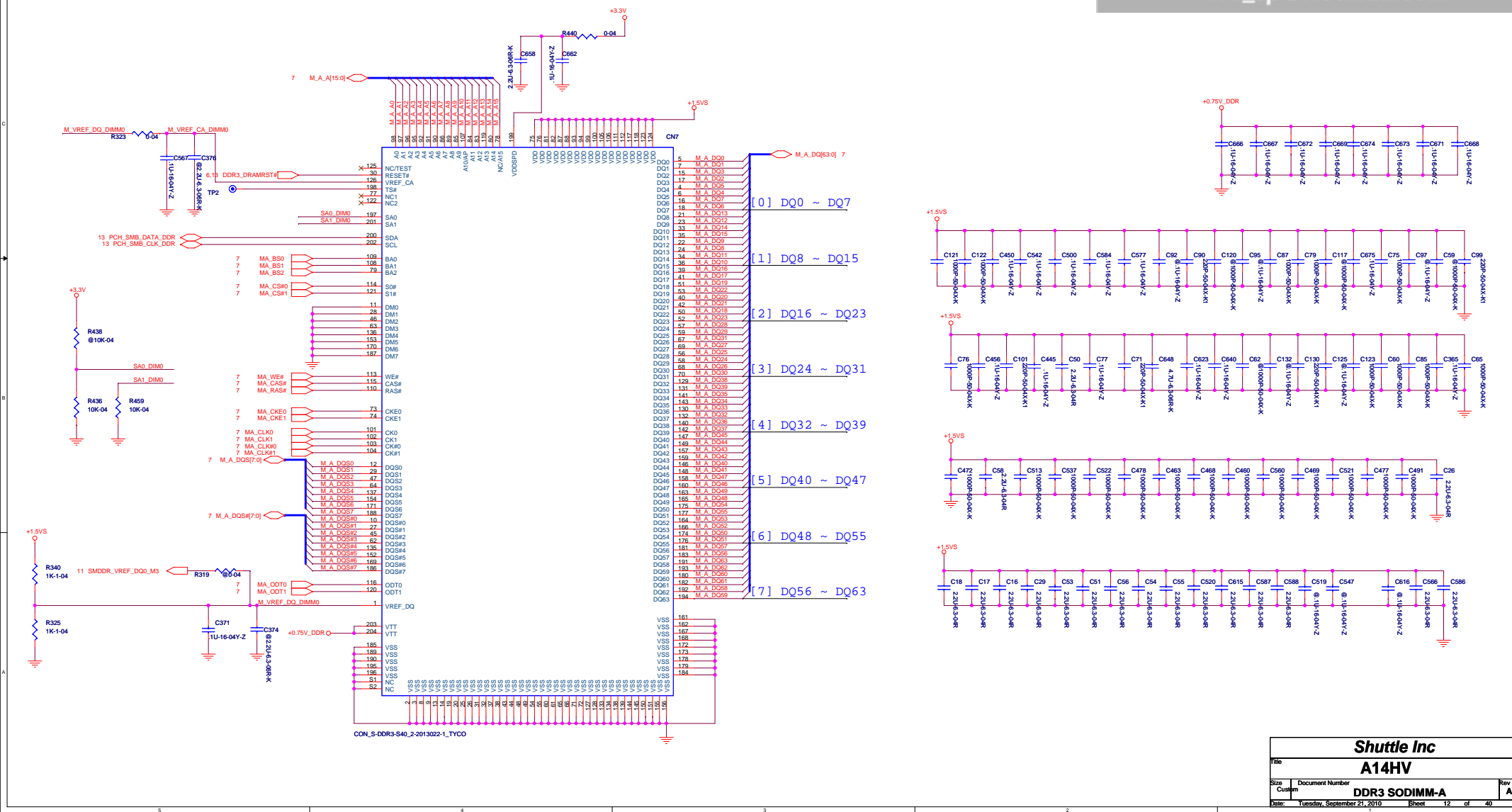


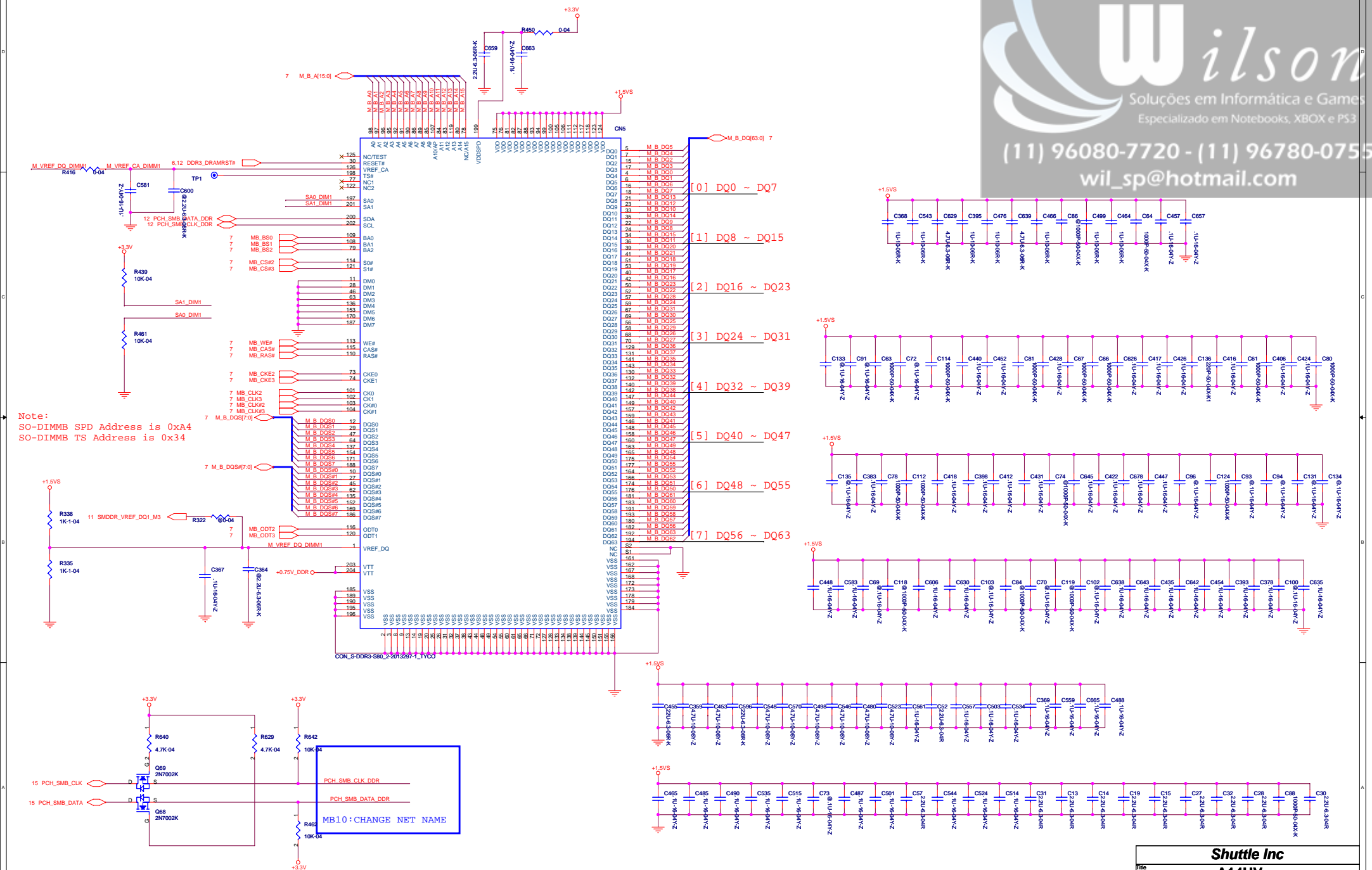
On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V



MB6:ADD 0R FOR VCCSA SENSOR

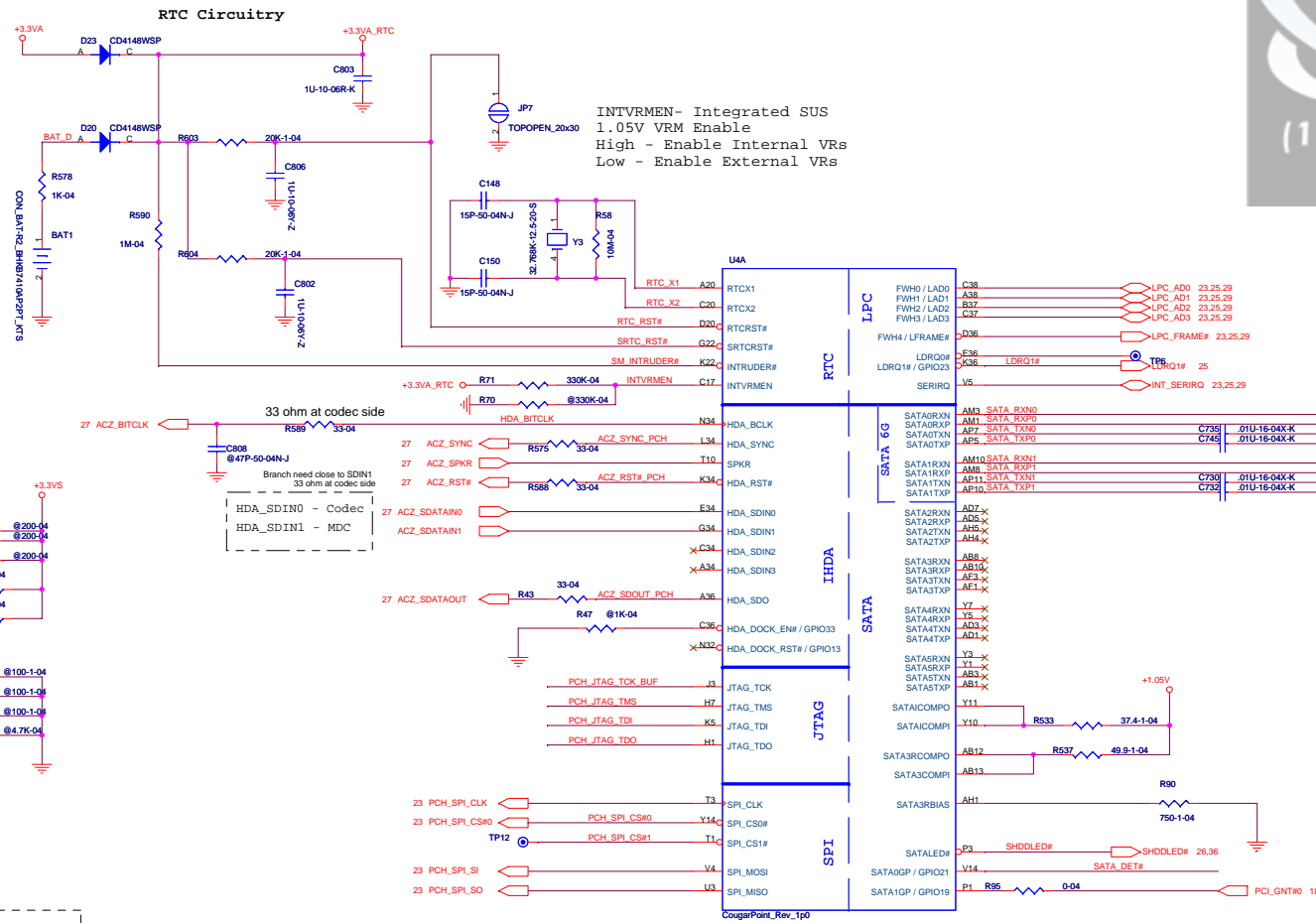




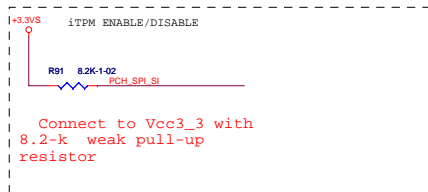
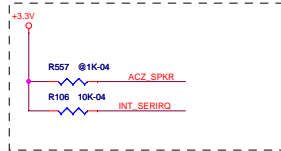
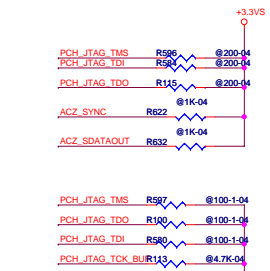
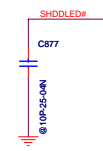
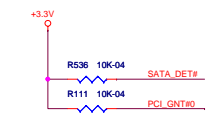


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Cougar Point Chipset (RTC,LPC,SATA,HDA,SPI,JTAG)



SATA[x]GP pins if unused require 8.2-k to 10-k pull-up to +Vcc3_3 or 8.2-k to 10-k pull-down to ground.

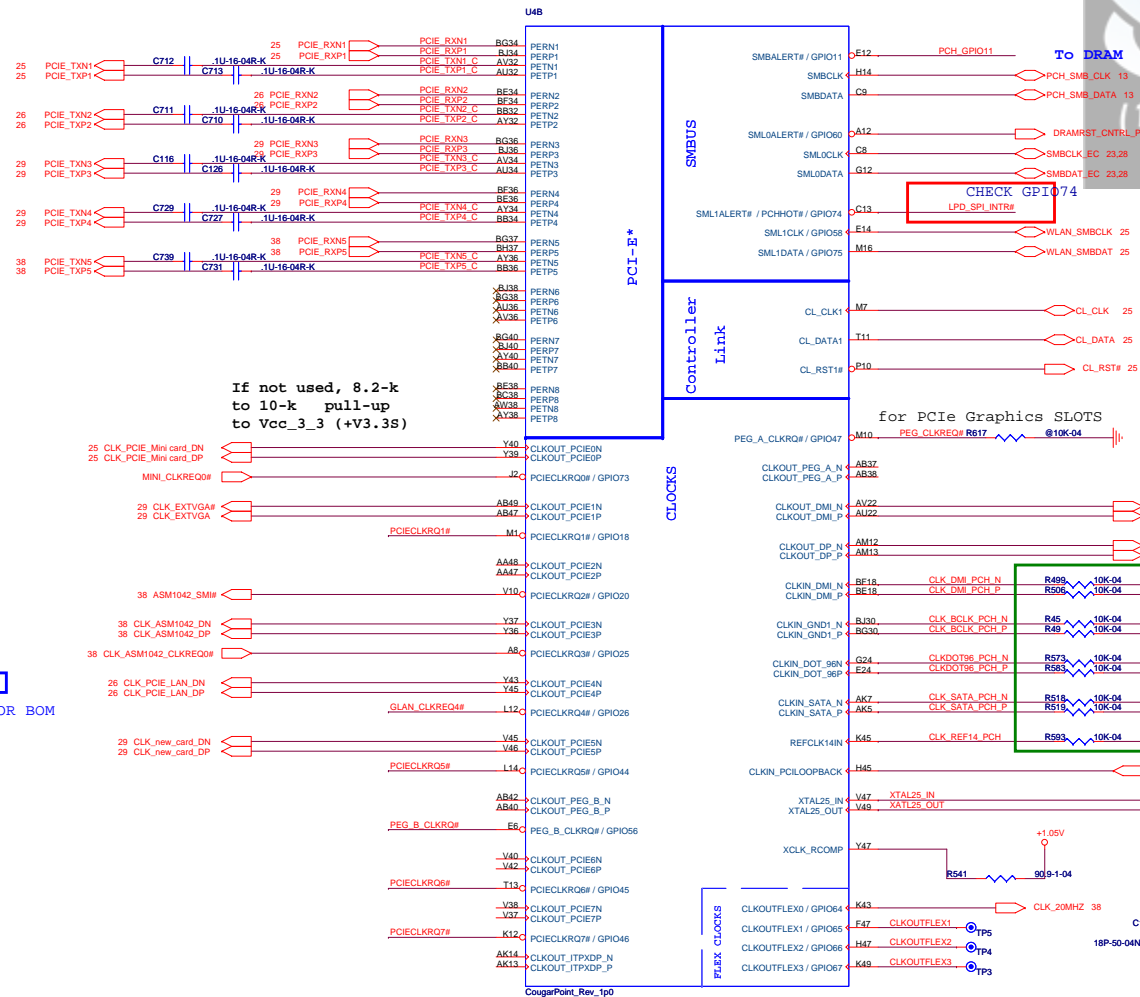


GPI033: This signal should be connected to the reset signal of the CODEC in the dock Station. This can be left unconnected when not in use.

Cougar Point Chipset (PCIE,SMBUS,CLOCK)

PCIE	Location
PCIE 1	CN3 (MINI CARD CONN)
PCIE 2	U4 (LAN)
PCIE 3	CN1 (NEW COAD & TV CARD)
PCIE 4	CN1 (NEW COAD & TV CARD)
PCIE 5	U13 (USB 3.0 ASM1042)

CLK	Location
CLK 0	CN3 (MINI CARD CONN)
CLK 1	CN1 (NEW COAD & TV CARD)
CLK 3	U13 (USB 3.0 ASM1042)
CLK 4	U4 (LAN)
CLK 5	CN1 (NEW COAD & TV CARD)



This input has to be terminated with a 10-kOhms pull-down termination resistor in Integrated Clock generation mode.

Cougar Point Chipset (DMI,FDI)



DSWODVREN - On Die DSW VR Enable

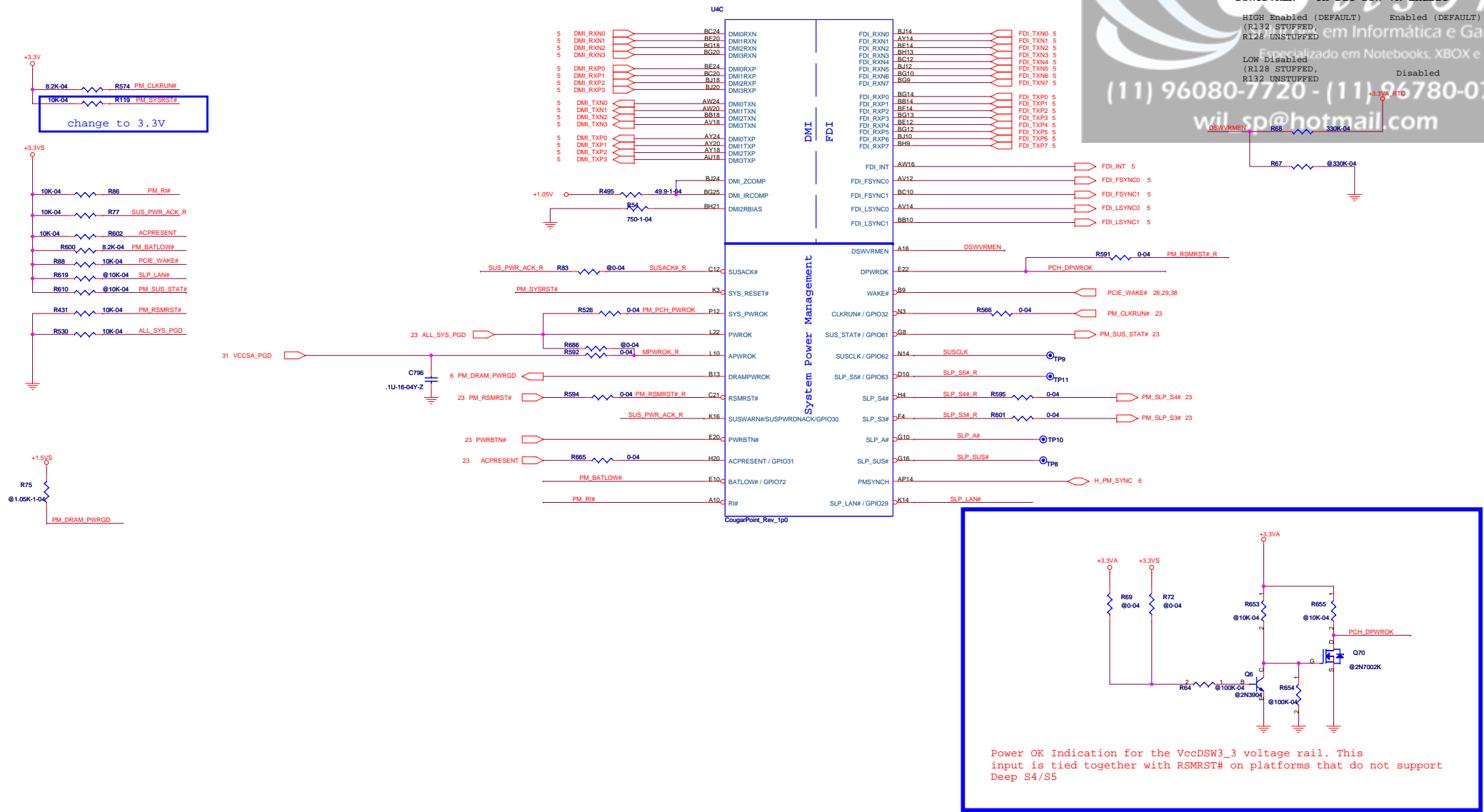
HIGH Enabled (DEFAULT) Enabled (DEFAULT)
(R132 STUFFED, R128 UNSTUFFED)

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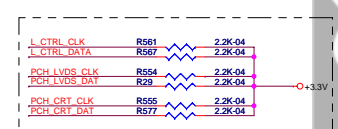
LOW Disabled
(R128 STUFFED, R132 UNSTUFFED)

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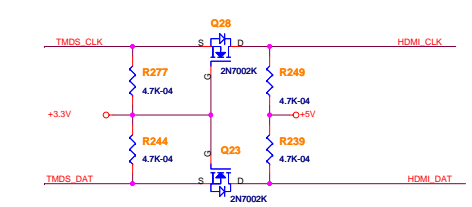
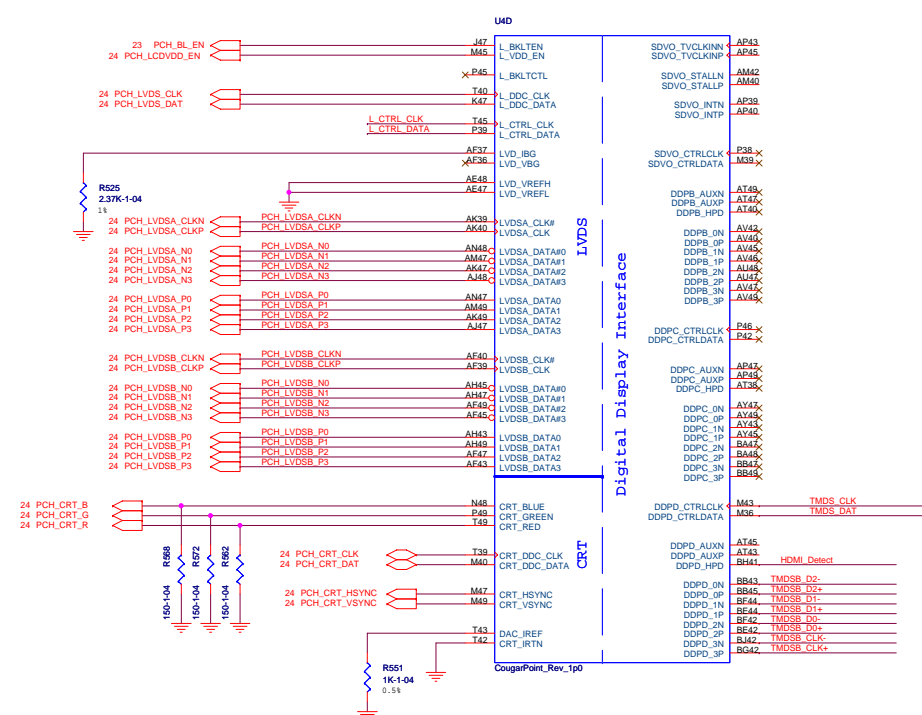


Cougar Point Chipset (LVDS,CRT,Digital Display)

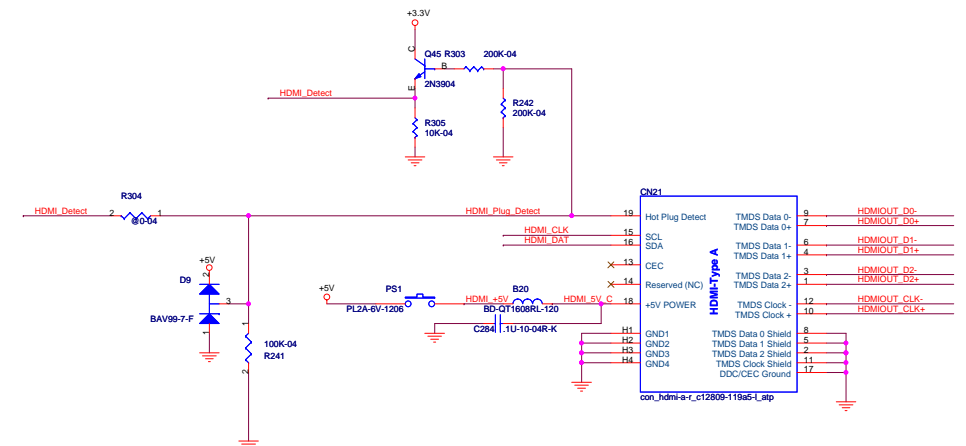
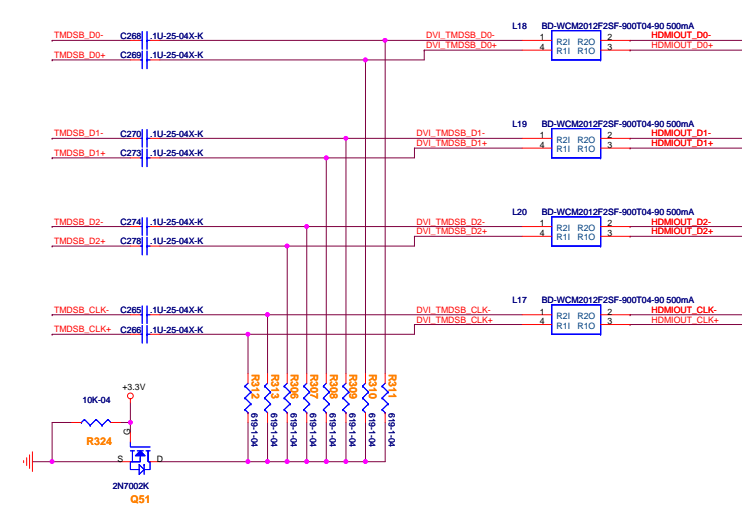


Configuration Wise Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	DisplayPort ¹ Mapping	HDMI/DVI Mapping
PORT-B	DDPB_00P	SDVO_RED	DDPB_00P	TMDSB_DATA2
	DDPB_00N	SDVO_RED#	DDPB_00N	TMDSB_DATA2#
	DDPB_01P	SDVO_GREEN	DDPB_01P	TMDSB_DATA1
	DDPB_01N	SDVO_GREEN#	DDPB_01N	TMDSB_DATA1#
	DDPB_02P	SDVO_BLUE	DDPB_02P	TMDSB_DATA0
	DDPB_02N	SDVO_BLUE#	DDPB_02N	TMDSB_DATA0#
	DDPB_03P	SDVO_CLK	DDPB_03P	TMDSB_CLK
	DDPB_03N	SDVO_CLK#	DDPB_03N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMI0_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMI0_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMI0_CTRLDATA



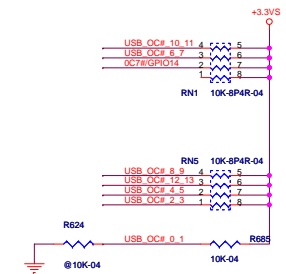
CHECK HDMI SPEC AND CRB



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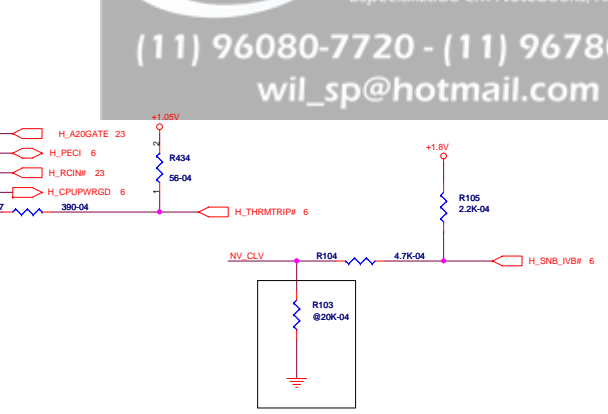
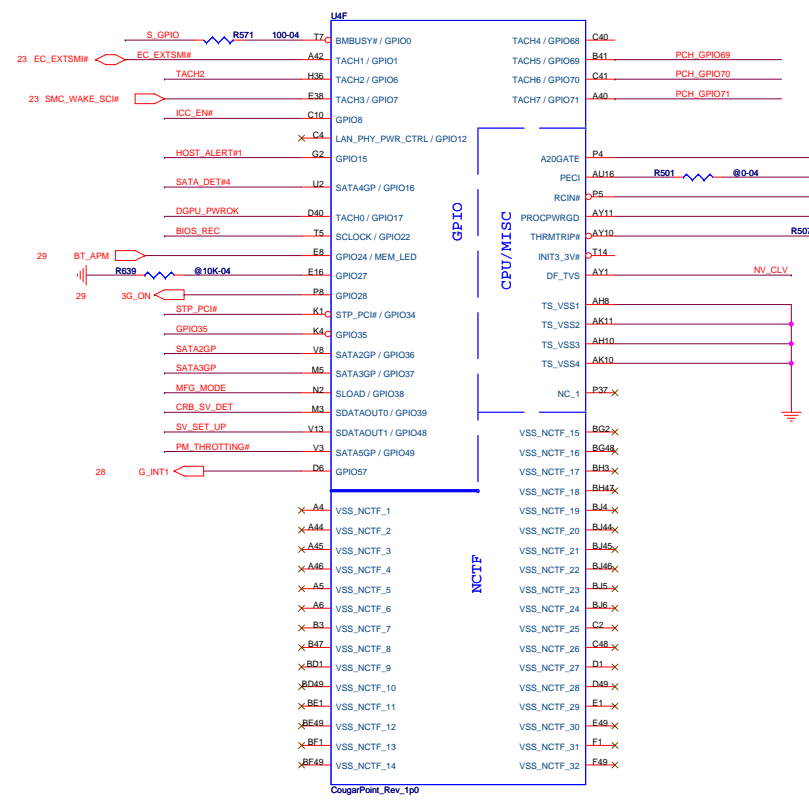
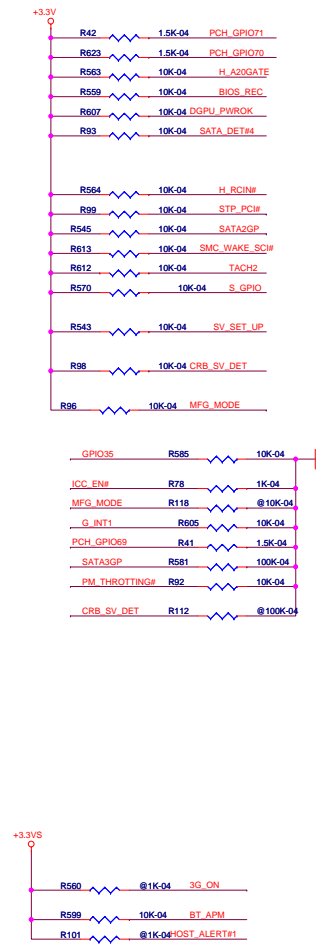
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U0H		
H5	VSS[0]	
AA17	VSS[1]	AK39
AA2	VSS[2]	AK4
AA3	VSS[3]	AK42
AA33	VSS[4]	AK46
AA34	VSS[5]	AK8
AB11	VSS[6]	AL16
AB14	VSS[7]	AL17
AB39	VSS[8]	AL19
AB4	VSS[9]	AL2
AB43	VSS[10]	AL21
AB5	VSS[11]	AL23
AB7	VSS[12]	AL26
AC19	VSS[13]	AL27
AC2	VSS[14]	AL31
AC21	VSS[15]	AL33
AC24	VSS[16]	AL34
AC33	VSS[17]	AL48
AC34	VSS[18]	AM11
AC48	VSS[19]	AM14
AD10	VSS[20]	AM36
AD11	VSS[21]	AM39
AD12	VSS[22]	AM43
AD13	VSS[23]	AM45
AD19	VSS[24]	AM46
AD24	VSS[25]	AM7
AD26	VSS[26]	AN2
AD27	VSS[27]	AN29
AD33	VSS[28]	AN3
AD34	VSS[29]	AN31
AD36	VSS[30]	AP12
AD37	VSS[31]	AP19
AD39	VSS[32]	AP28
AD4	VSS[33]	AP30
AD40	VSS[34]	AP32
AD42	VSS[35]	AP38
AD43	VSS[36]	AP4
AD43	VSS[37]	AP42
AD46	VSS[38]	AP46
AD46	VSS[39]	AP8
AD8	VSS[40]	AR2
AE2	VSS[41]	AR48
AE3	VSS[42]	AT11
AF10	VSS[43]	AT13
AF12	VSS[44]	AT18
AD14	VSS[45]	AT22
AD16	VSS[46]	AT26
AE16	VSS[47]	AT28
AE18	VSS[48]	AT30
AE24	VSS[49]	AT32
AF26	VSS[50]	AT34
AF27	VSS[51]	AT39
AF29	VSS[52]	AT42
AF31	VSS[53]	AT46
AF39	VSS[54]	AT7
AF4	VSS[55]	AU24
AF42	VSS[56]	AU30
AF46	VSS[57]	AV16
AF5	VSS[58]	AV20
AF7	VSS[59]	AV24
AF8	VSS[60]	AV30
AG19	VSS[61]	AV38
AG2	VSS[62]	AV4
AG31	VSS[63]	AV43
AG48	VSS[64]	AV8
AH11	VSS[65]	AW14
AH3	VSS[66]	AW18
AH36	VSS[67]	AW2
AH39	VSS[68]	AW22
AH40	VSS[69]	AW26
AH42	VSS[70]	AW28
AH46	VSS[71]	AW32
AH7	VSS[72]	AW34
AJ19	VSS[73]	AW36
AJ21	VSS[74]	AW40
AJ30	VSS[75]	AW48
AJ33	VSS[76]	AX11
AJ34	VSS[77]	AY22
AK12	VSS[78]	AY28
AK3	VSS[79]	

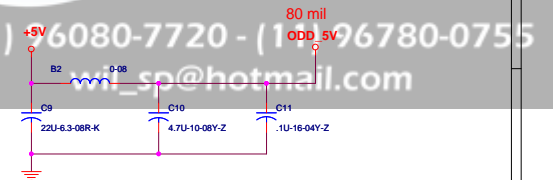
CougarPoint_Rev_1p0

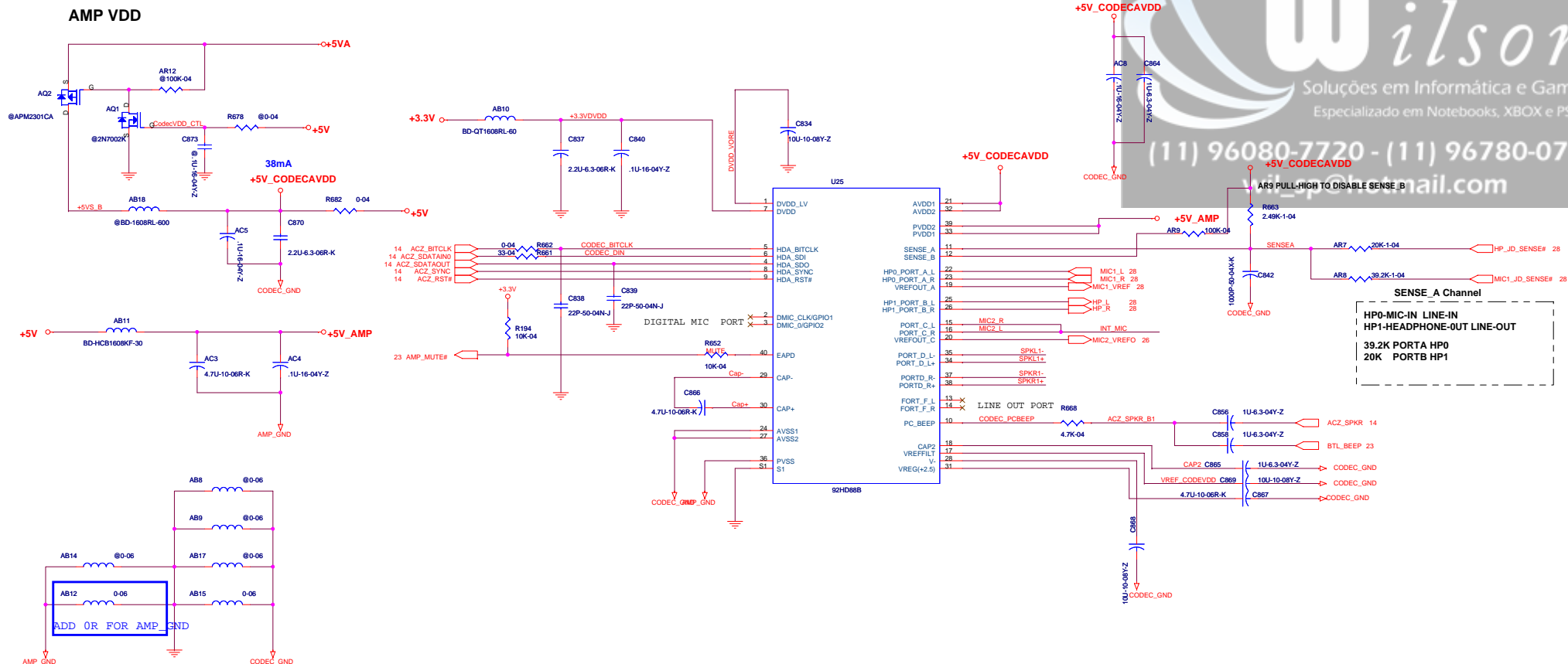
U0I		
AYA	VSS[159]	H46
AY42	VSS[160]	K18
AY46	VSS[161]	K26
AY48	VSS[162]	K39
B11	VSS[163]	K7
B19	VSS[164]	K46
B21	VSS[165]	L18
B23	VSS[166]	L2
B27	VSS[167]	L20
B31	VSS[168]	L28
B35	VSS[169]	L38
B39	VSS[170]	L46
B7	VSS[171]	M12
F45	VSS[172]	M16
BB12	VSS[173]	M22
BB16	VSS[174]	M24
BB20	VSS[175]	M30
BB22	VSS[176]	M32
BB24	VSS[177]	M34
BB28	VSS[178]	M38
BB30	VSS[179]	M42
BB36	VSS[180]	M46
BB4	VSS[181]	N18
BC14	VSS[182]	N19
BC16	VSS[183]	N30
BC2	VSS[184]	N47
BC22	VSS[185]	P11
BC26	VSS[186]	P18
BC30	VSS[187]	P30
BC36	VSS[188]	P40
BC40	VSS[189]	P43
BC42	VSS[190]	P7
BC46	VSS[191]	P8
BD46	VSS[192]	P22
BD8	VSS[193]	P48
BE22	VSS[194]	T11
BE26	VSS[195]	T37
BE40	VSS[196]	T4
BE46	VSS[197]	W34
BE10	VSS[198]	T46
BE12	VSS[199]	T8
BE16	VSS[200]	V11
BF10	VSS[201]	V17
BF20	VSS[202]	V26
BF24	VSS[203]	V29
BF26	VSS[204]	V31
BF28	VSS[205]	V36
BF30	VSS[206]	V39
BF32	VSS[207]	V43
BF34	VSS[208]	V7
BF36	VSS[209]	W17
BF40	VSS[210]	W2
BFA	VSS[211]	W27
BG17	VSS[212]	W48
BG21	VSS[213]	Y12
BG33	VSS[214]	Y38
BG44	VSS[215]	Y4
BG8	VSS[216]	Y42
BH11	VSS[217]	Y46
BH15	VSS[218]	Y8
BH19	VSS[219]	BG29
BH20	VSS[220]	N24
BH21	VSS[221]	AI3
BH27	VSS[222]	AD47
BH31	VSS[223]	B43
BH33	VSS[224]	BE10
BH36	VSS[225]	BG41
BH39	VSS[226]	G14
BH43	VSS[227]	H16
BH7	VSS[228]	T36
D11	VSS[229]	BG22
D12	VSS[230]	BG24
D16	VSS[231]	C22
D18	VSS[232]	AP13
D22	VSS[233]	M14
D24	VSS[234]	AP3
D26	VSS[235]	AP1
D30	VSS[236]	BE16
D32	VSS[237]	BC16
D34	VSS[238]	BG28
D36	VSS[239]	BU28
D38	VSS[240]	
D42	VSS[241]	
D8	VSS[242]	
E18	VSS[243]	
E26	VSS[244]	
G18	VSS[245]	
G20	VSS[246]	
G26	VSS[247]	
G28	VSS[248]	
G36	VSS[249]	
G46	VSS[250]	
H12	VSS[251]	
H18	VSS[252]	
H22	VSS[253]	
H24	VSS[254]	
H26	VSS[255]	
H30	VSS[256]	
H32	VSS[257]	
H34	VSS[258]	
F3		

CougarPoint_Rev_1p0

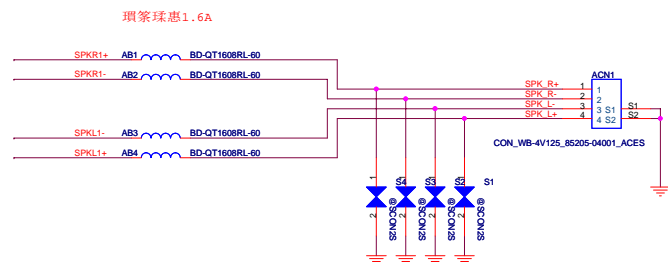
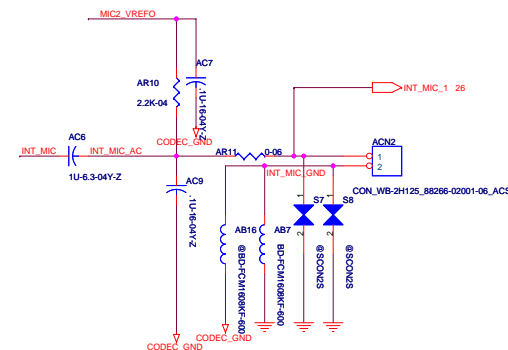
[illegible]

CON_ODD_43SR_1759838-6_TYCO

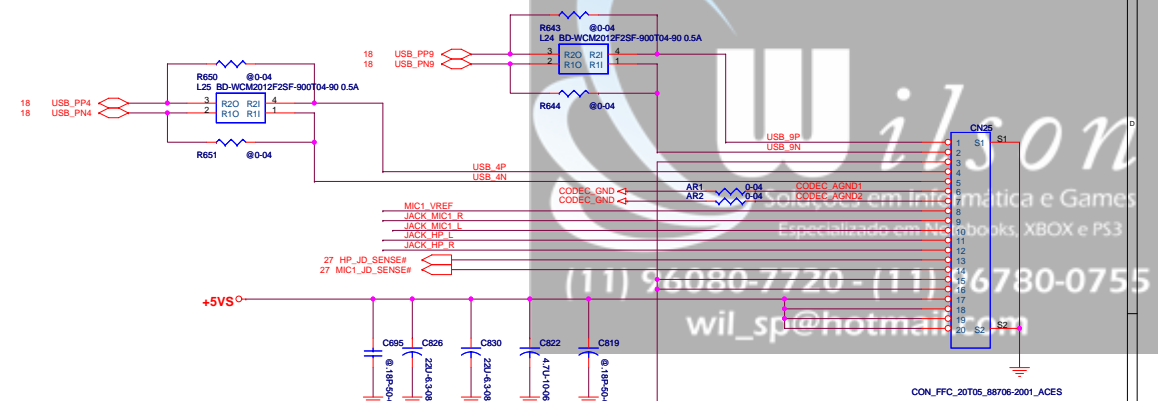
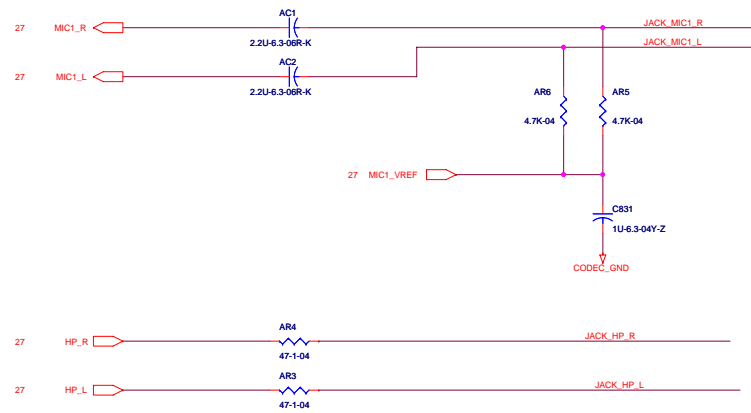
[illegible]

CODEC 92HD81

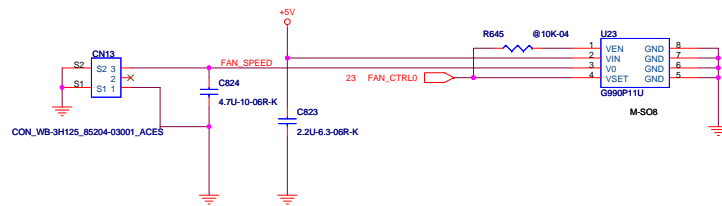
INT_SPEAKER

**INT_MIC**

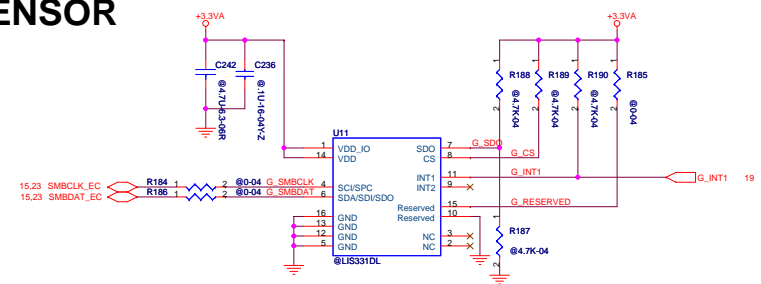
FAN CONTROLLER



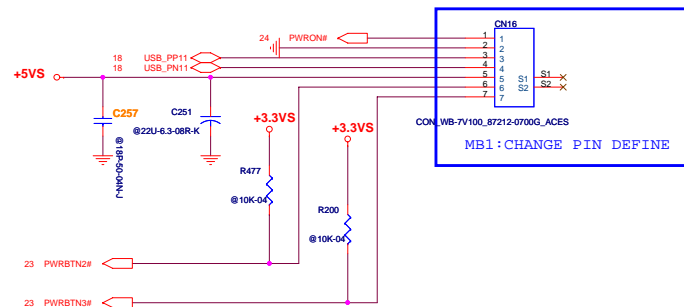
FAN CONTROLLER



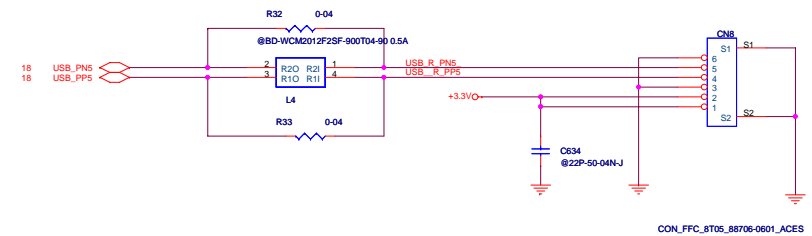
G-SENSOR



EXT USB PORT 4

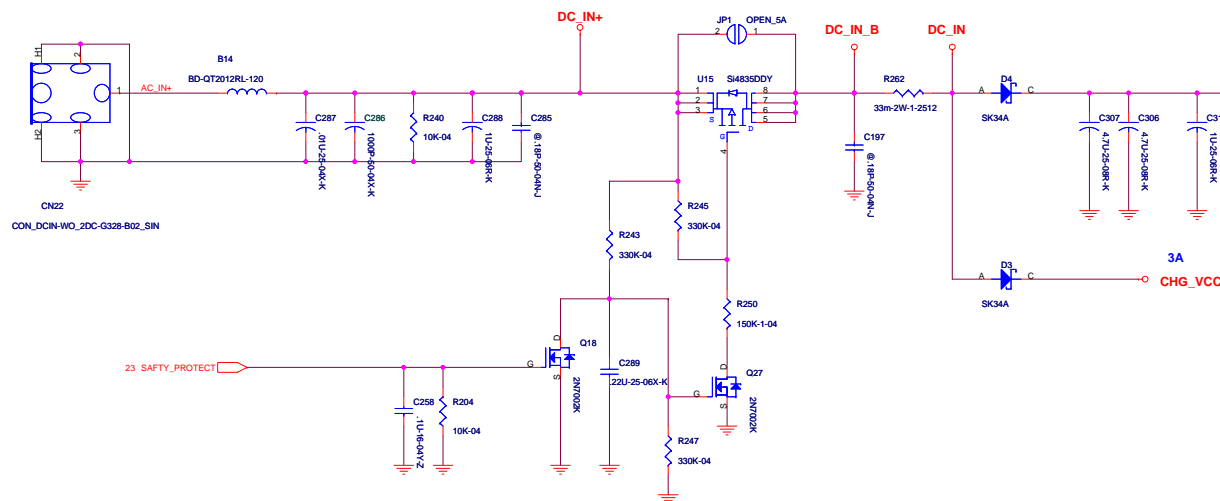


FingerPrint

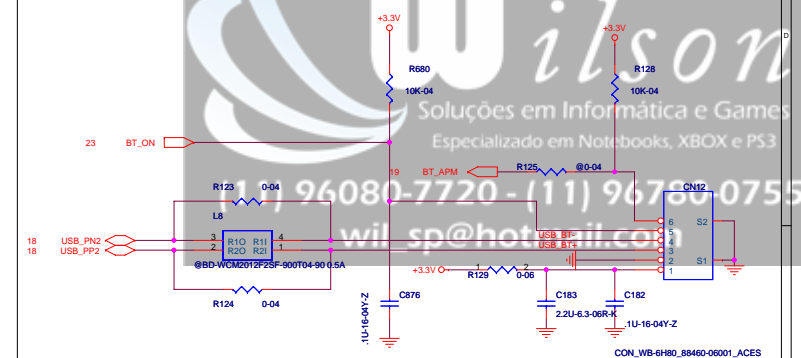


DC IN

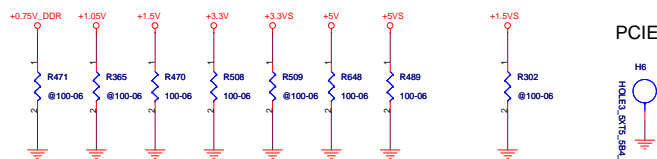
PROJECT	A14HM02		
Adaptor	65W	90W	120W
Rsense	33m Ohm	25m Ohm	18m Ohm
Stop Charger	60W	80W	110W



BT CONN



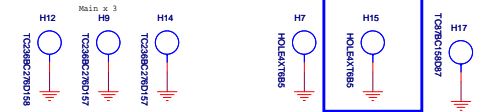
Discharge Resistor



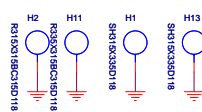
PCIE



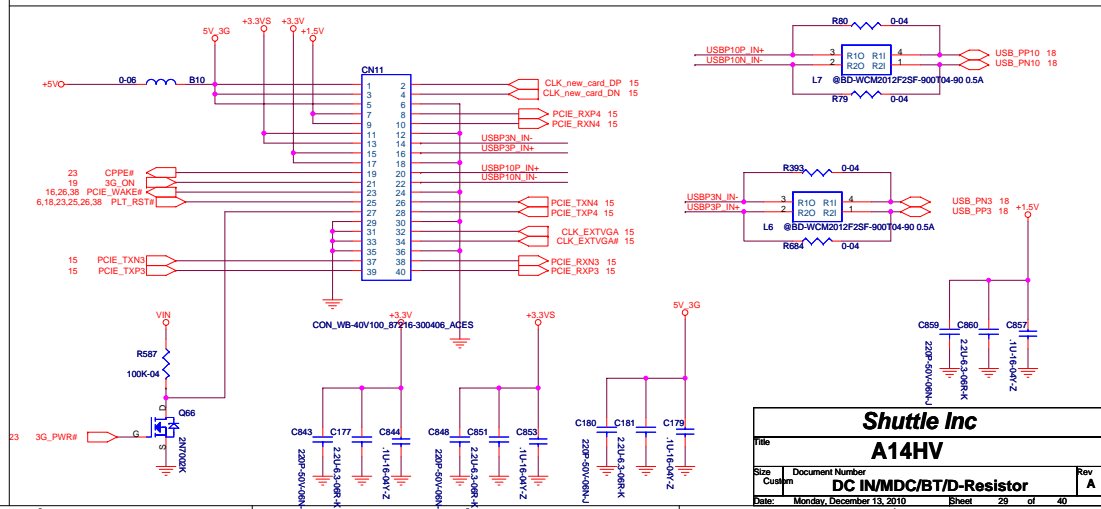
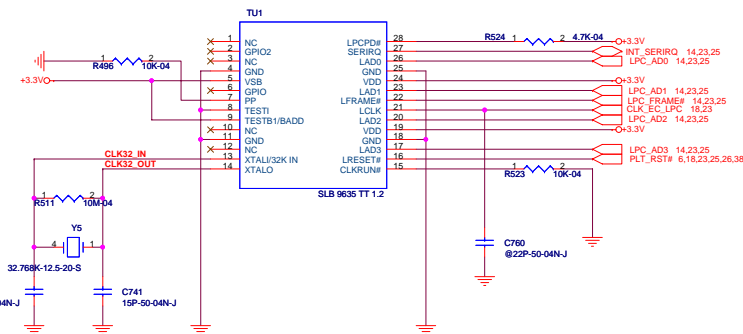
Thermal Module



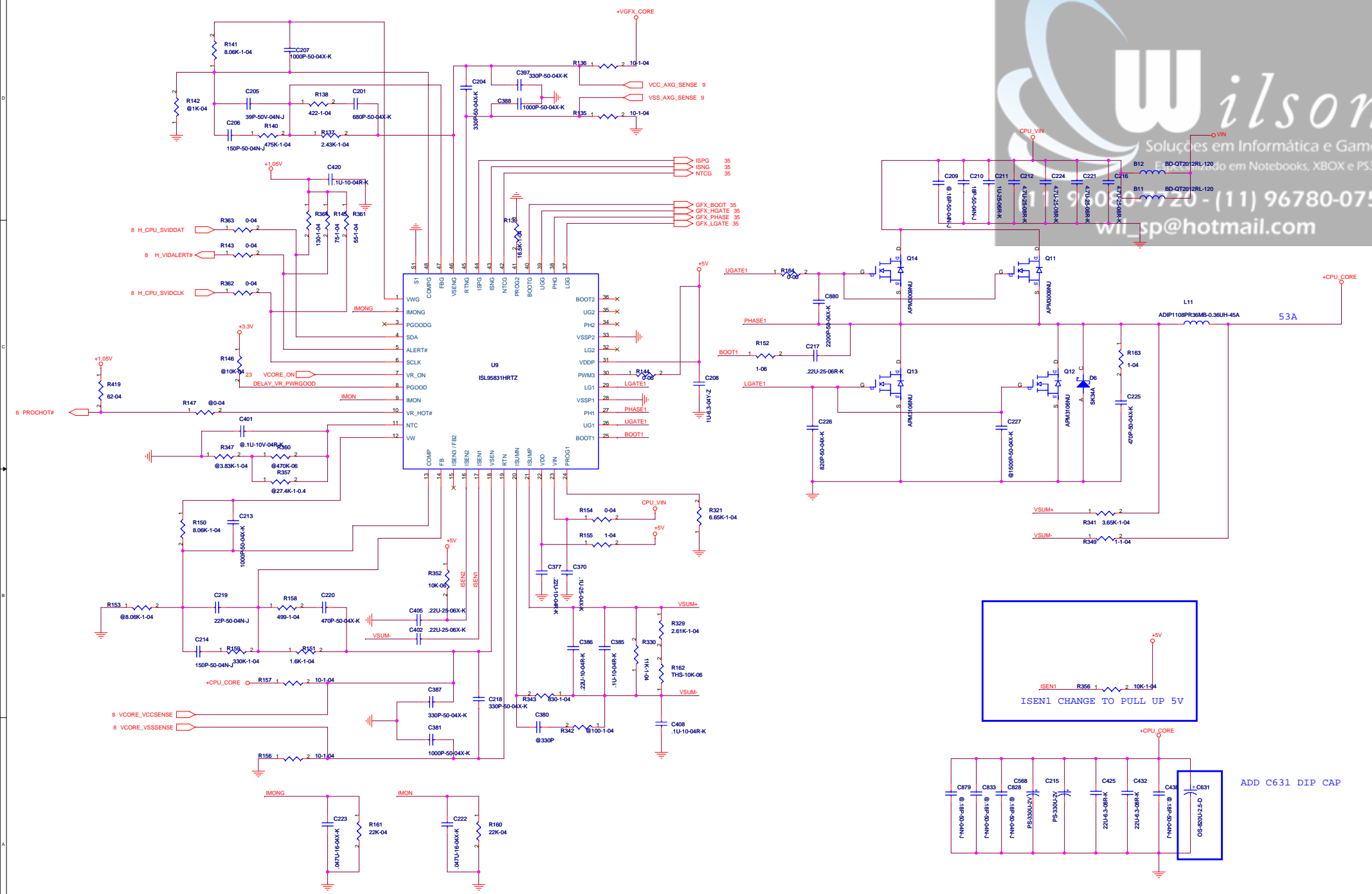
い 稚 び 錠



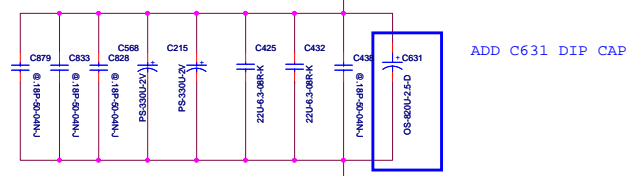
TPM

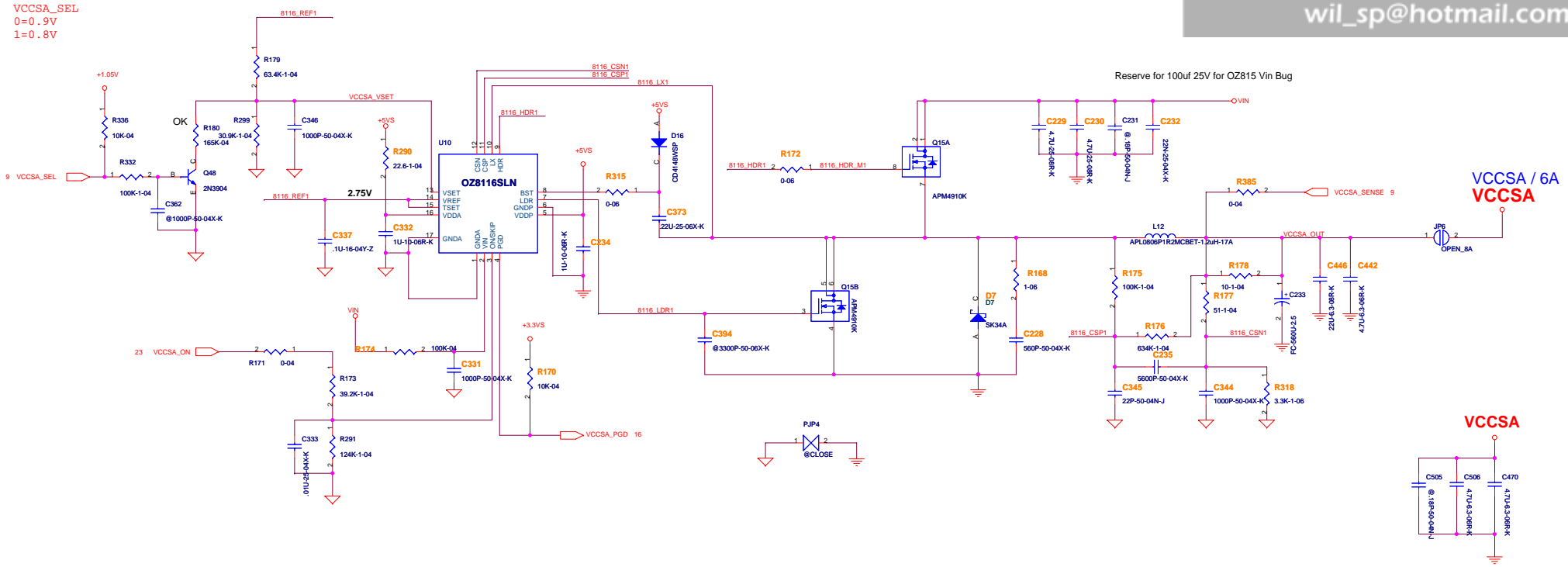


Shuttle Inc		
A14HV		
Title	Document Number	Rev
Size	Custm	A
DC IN/MDC/BT/D-Resistor		
Date	Monday, December 13, 2010	Sheet 29 of 40



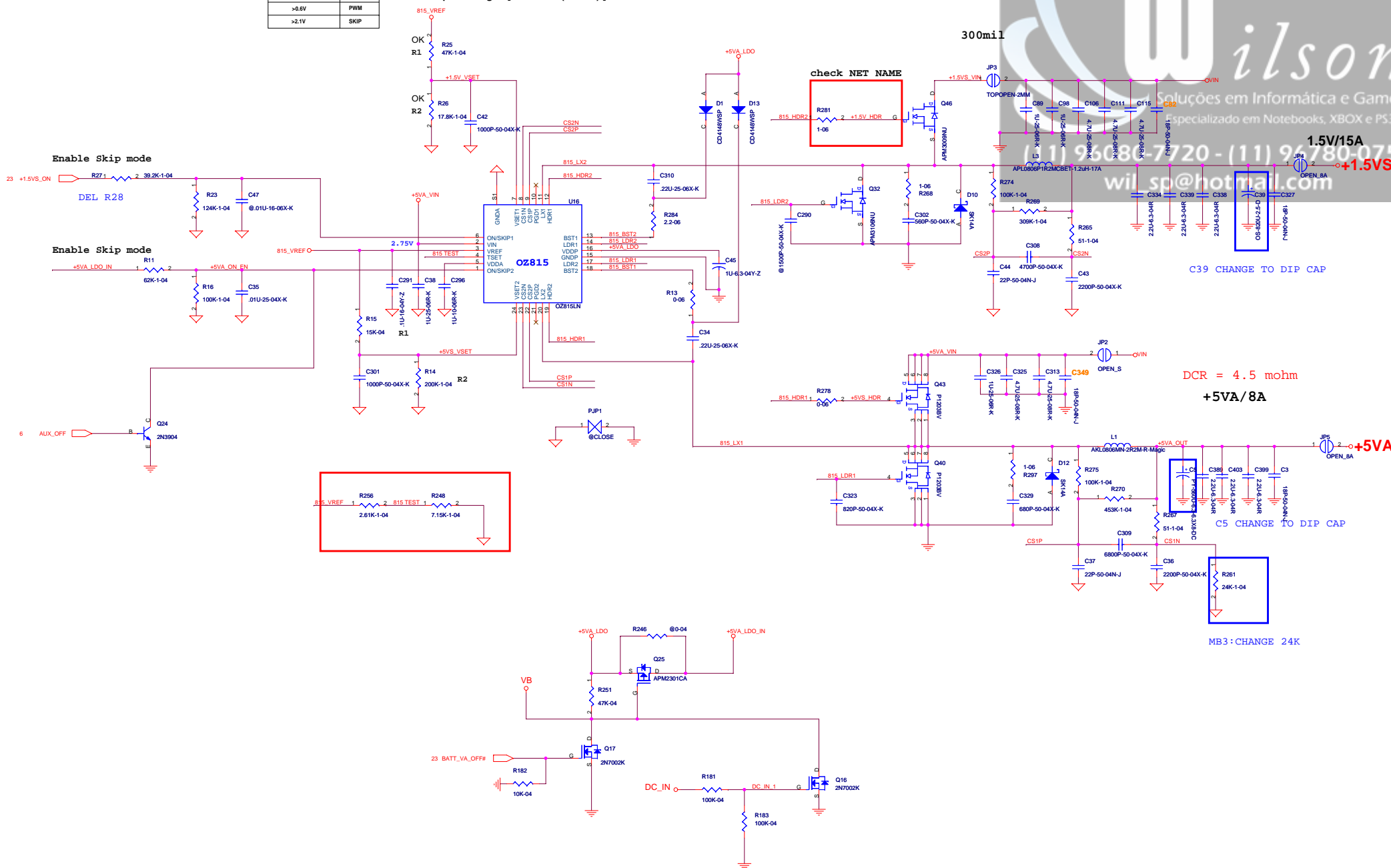
ISEN1 CHANGE TO PULL UP 5V





+1.8V/+5V_ON Voltage	Mode
<0.4V	OFF
>0.6V	PWM
>2.1V	SKIP

$$\text{Output Voltage} = \left[\frac{V_{\text{ref}} \times R2}{R1 + R2} \right] \times 2$$



Shuttle Inc			
A14HV			
Title	Document Number	Rev	
Size	Custm	+1.05VS/+5VA (OZ815)	A
Date	Friday, December 03, 2010	Sheet	33 of 40

CHARGER

CHG_VCC O

C165 @180P-50-04X-K

C176 @1000P-50-04X-K

C164 4.7U-25-06R-K

C198 1U-25-06R-K

C200 .22U-25-06X-K

C312 1U-25-06R-K

C322 1U-25-06R-K

C294 1000P-50-04X-K

C316 1U-25-06R-K

C317 1U-25-06R-K

C318 1U-25-06R-K

C335 2200P-50-04X-K

R273 10-1-06

R272 10-1-06

R296 330-04

R295 20K-1-04

R257 270-1-06

R255 100K-04

R263 107K-1-04

R252 56K-1-04

R276 56K-1-04

R51 20K-1-04

R288 100K-04

R223 1K-04

R57 100-1-04

R55 100-1-04

R282 10-1-06

R281 25m-1-2512

R280 100m-1w-1-2512

R279 10-1-06

R278 10-1-06

R277 10-1-06

R276 10-1-06

R275 10-1-06

R274 10-1-06

R273 10-1-06

R272 10-1-06

R271 10-1-06

R270 10-1-06

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R93 10-1-06

R92 10-1-06

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R90 10-1-06

R89 10-1-06

R88 10-1-06

R87 10-1-06

R86 10-1-06

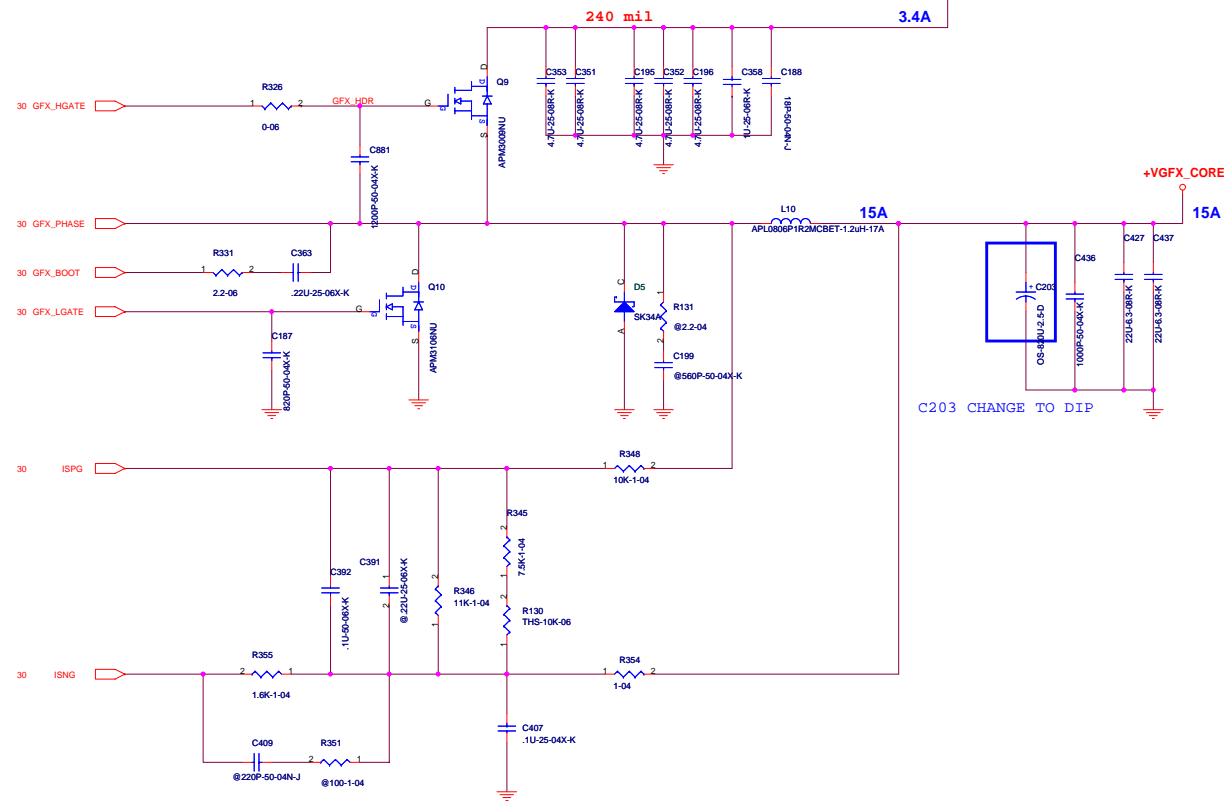
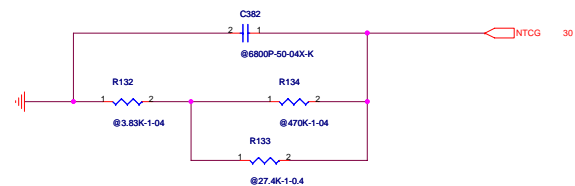
R85 10-1-06

R84 10-1-06

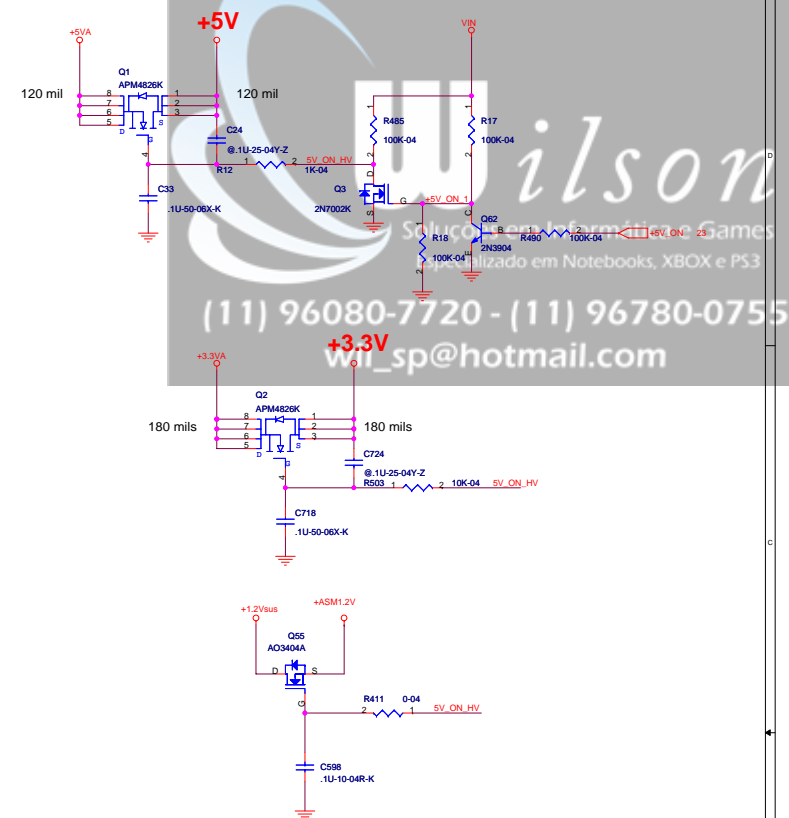
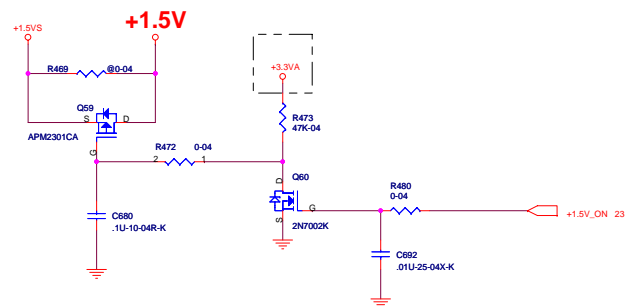
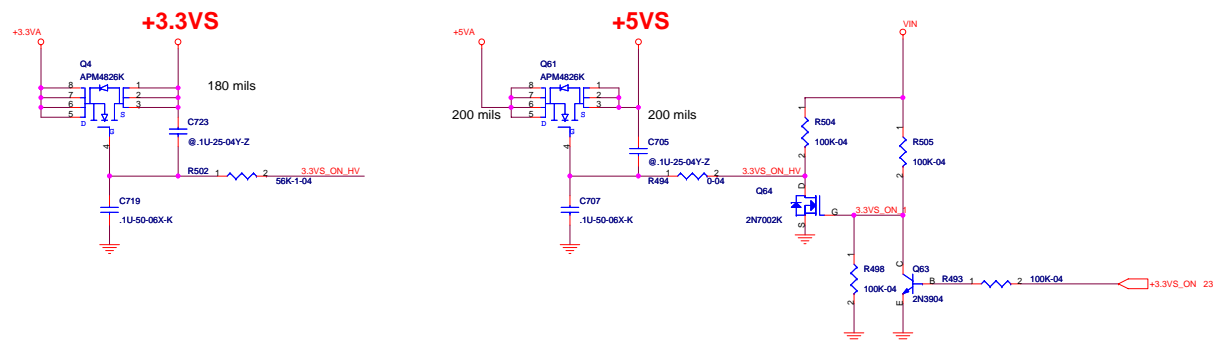
R83 10-1-06

R82 10

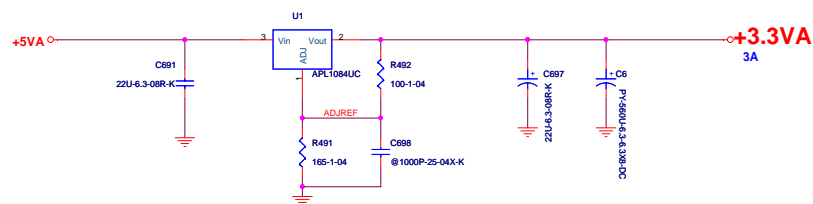
$17.6V \rightarrow BAT_V = 2.2V$
 $16.8V \rightarrow BAT_V = 2.1V$
 $13.2V \rightarrow BAT_V = 1.65V$
 $12.6V \rightarrow BAT_V = 1.575V$
 $9.0V \rightarrow BAT_V = 1.125V$



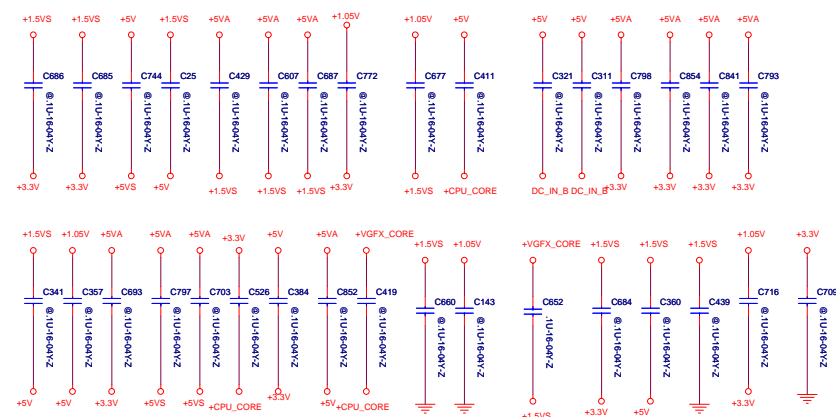
VCCSW



LDO



HIGH-SPEED CAP



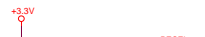
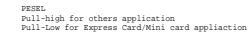
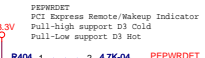
USB3.0



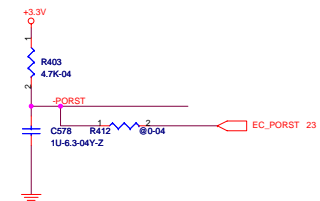
GP100	GP101	GP102	Function
1	1	0	Synchronous Mode
1	1	1	Asynchronous Mode (default)
0	0	x	Debug/Test Mode

* GP100 GP101 GP102 internal Pull-high

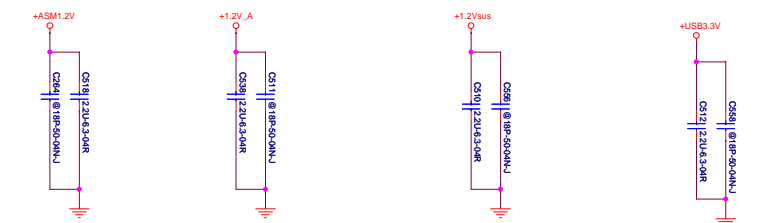
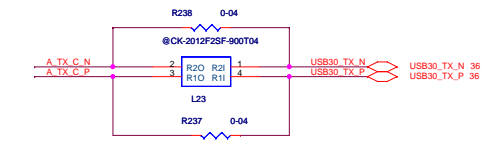
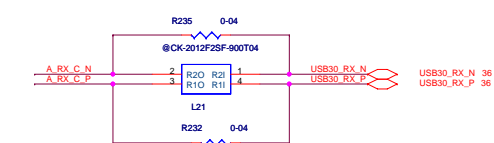
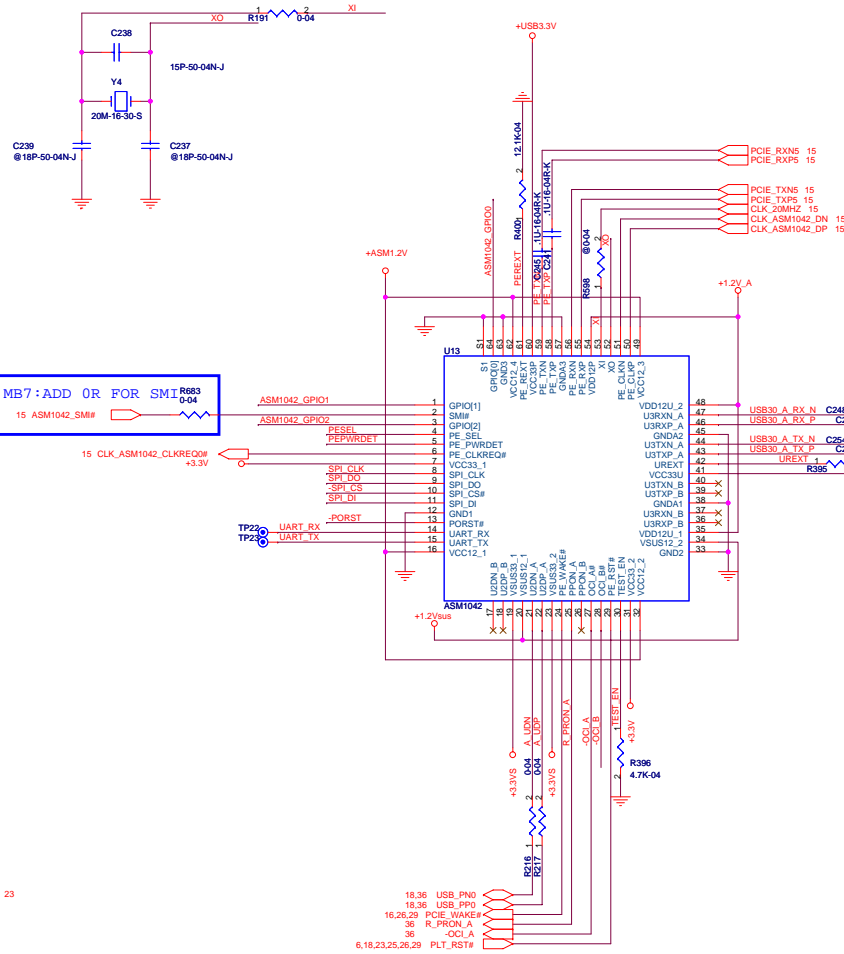
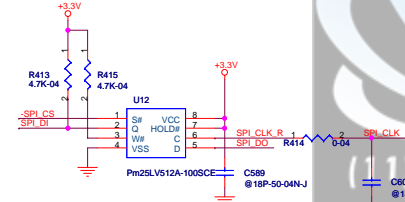
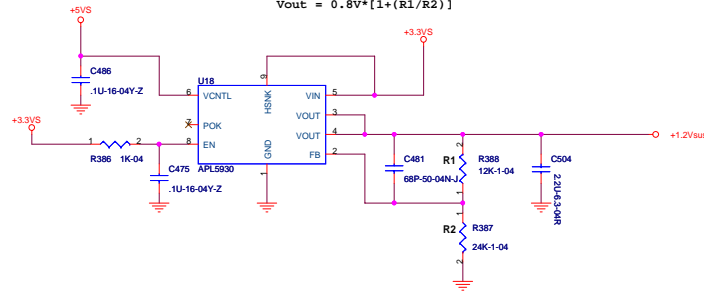
ASM1042	USB3.0	USB3.0
Clock Source	480MHz	1000MHz from PCIe CLK
Sync	200MHz X'tal	200MHz X'tal (For PCIe over clock)



Must meet Power Sequence Spec.



$$V_{out} = 0.8V \cdot [1 + (R1/R2)]$$



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Shuttle Inc			
Title			
A14HV			
Size	Document Number		Rev
Custom	History		A
Date:	Tuesday, September 21, 2010	Sheet	40 of 40
1			